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Simulation of the Electrical Characteristics of Double Gate FinFET with the Variation of Channel Length

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ABSTRACT

In this research work, electrical characteristics of double gate FinFET have been simulated by varying the length of the channel region. 40 nm, 50nm and 60nm channel length has been considered to simulate the drain current VS front gate voltage characteristics for FinFET. For these three different values of channel length, electric field profile along the FinFET channel has also been studied in this research. Finally the electrostatic potential along the channel has been simulated for varying the channel length of the FinFET. After analyzing the simulations, it has been proposed that higher drain current, wide variation of electric field along the channel region as well as increased carrier mobility and lower electrostatic potential along the channel can be achieved for smaller value of the channel length of FinFET. The whole simulation works have been performed by Nano HUB online simulation tool named "DG-MOSFET" where the data of the simulation were processed and the plots were generated.

Keywords: FinFET, Nano HUB onlive, DG-MOSFET

1. Introduction

Scaling of Bulk CMOS technology is approaching to the limit because the continuing scaling of CMOS (Complementary Metal-Oxide-Semiconductor) technology requires noteworthy innovations in different fields, from short channel effect restraint to carrier transport improvement. So Double-gate (DG) MOSFETs such as FinFET have been considered to be the ultimately scalable CMOS technology due to their better immunity to short channel effect (SCE), better current drive and almost ideal subthre shold slope[1][2]. As devices shrinking further, the problems with the planar or bulk Si-CMOS technology are increasing. Several short channel effects like V_T roll off, drain induced barrier lowering (DIBL), increasing leakage currents such as subthre shold S/D leakage, gate induced drain leakage (GIDL), gate direct tunneling leakage, and hot carrier effects produced in the devices which degrading the use in industry. These exclusive qualities and electrical properties of FinFET motivated us to perform some simulation based research on FinFET by varying some of the electrical and electronic parameters of this device. Channel length and channel material play very important role in the exclusive electrical properties of FinFET. In this research work, the electrical characteristics of FinFET has been simulated with varying the length of wrapped channel region. Firstly, the drain current VS from gate voltage of the FinFET has been simulated with varying the channel length. Then the electric field profile along the channel of the FinFET has been studied and simulated for different values of channel length. After that, the profile of electrostatic potential in the wrapped channel region of the FinFET has been studied with varying the channel length.

2. FinFET device structure and current-voltage relationships

For the efficient solution of the problems caused by MOSFET like threshold voltage roll off, drain induced barrier lowering (DIBL), increasing leakage current etc, double Gate MOSFET, called FinFET has been introduced [3][4]. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the gate of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device [5]. The structure of the FinFET device considered for this research work is shown in Fig. 1 and the FinFET structure, with oxide layer thickness and channel width are shown in Fig. 2.

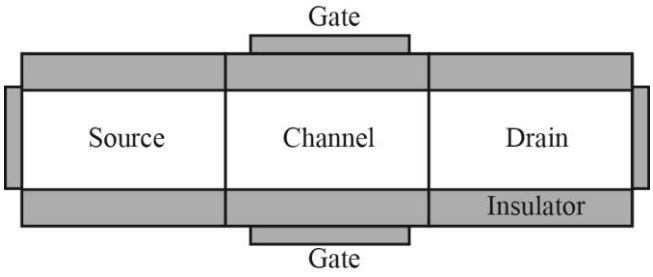

Fig. 1: Structure of double gate FinFET structure

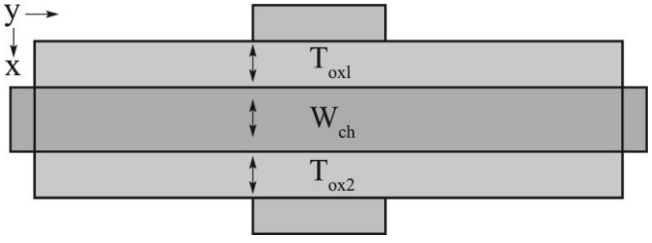

Fig. 2: Structure of FinFET showing oxide layers

In the linear region of the I-V characteristics of FinFET, the relation of drain to source current I_{ds} with drain to source voltage v_{ds},dielectric constant for channel is 11.7 and for insulator is 3.9, for a given gate voltage v_g (> threshold voltage, v_t) is given bellow [6][7][8]:

$$I_{ds} = 2\mu C_{ox}\frac{W}{L}\left(v_g - v_t - \frac{v_{ds}}{2}\right)v_{ds}$$

Here, W/L is the device width to length ratio and $C_{ox}$is the gate oxide capacitance per unit area.

In the saturation region, the relation between I_{ds} with v_{ds} is given here [9]:

$$I_{ds} = \mu C_{ox}\frac{W}{L}\frac{(v_g - v_t)^2}{2m}$$

$$\text{Where, } m = 1 + \frac{3t_{ox}}{x_d}$$

Here, X_d is the depletion layer thickness and t_{ox} is the oxide thickness.

3. Simulations

Previous research work was performed to analyze the electrical characteristics variability like the variation of trans conductance with varying the gate voltage by changing the width of fin layer [10]. The variation of gate current has also been analyzed with varying gate voltage with the change of fin layer widthin that research work [10]. In this research work, we have analyzed the current-voltage characteristics of FinFET by varying the length of the channel of FinFET. Also, the electrical field profile along the fin channel has been studied here.

3.1 I-V Characteristics with varying Channel Length

The simulated *I-V* characteristics for double gate FinFET is shown in Fig.3, where channel length 40 nm has been considered. The generated curve of drain current VS front gate voltage of FINFET is quite similar of single gate MOSFET having 3 different regions: Linear region, Pinch off region and saturation region. But for high trans conductance of channel, low channel resistance and high on current, for a certain amount of gait voltage, large amount of drain current is obtained with a slight increase in drain voltage. This characteristics I-V curve shows two different curves for two drain voltage of 0.5 V and 1 V. For the slight increase of drain voltage, significant amount of increase in drain current is obtained in the curve.

The drain current *VS* front gate voltage of FinFET has been simulated for varying the channel length of the FinFET. Resistance of the channel increases with increasing the channel length. For the channel length of 50 nm, the *I-V* characteristics of FINFET has been simulated in Fig 4. From the figure, we observe that, the slope of the linear region of the curve has been decreased significantly from that of the curve for 40 nm channel length (previous fig.).

So, channel resistance has been greatly increased here and which makes the FinFET to reach to its pinch off region quickly. After that, for channel length of 60 nm, the *I-V* characteristics has been simulated again (shown in Fig-5) where the slope of the linear region again increased slightly than that for channel length 50 nm and again FinFET reaches to pinch off region quickly. All of these simulations have been performed for two drain voltages: 0.5V and 1 V.

Threshold voltage is not constant; it decreases linearly with increasing drain voltages. We have used 0.5 V and 1 V drain voltages. Itcan be assumed that, for 0.5 V drain voltage, threshold was 0.5 V and for 1 V drain voltage, threshold is nearly 0 V.

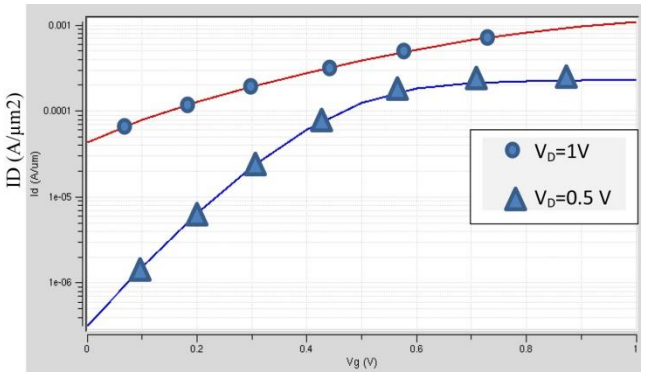

Fig. 3: Simulated I-V Characteristics for double gate FinFET for 40nm channel length

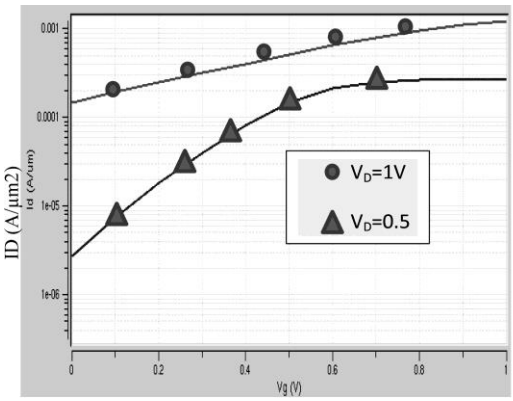

Fig. 4: Simulated I-V Characteristics for 50 nm Channel Length

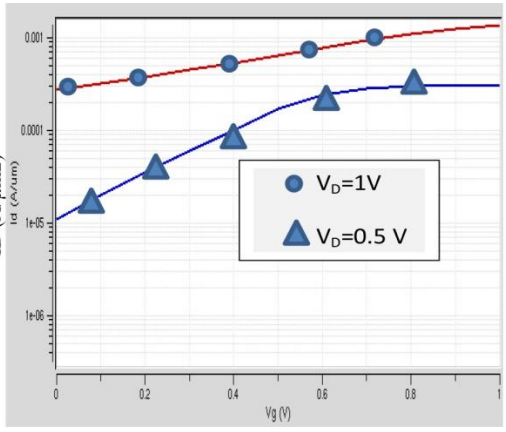

Fig. 5: Simulated I-V Characteristics for 60 nm Channel Length

3.2 Electric Field profile along the channel with varying Channel Length

The electric field profile of the FinFET has been studied in this simulation work with varying the channel length. For 40 nm, 50 nm and 60 nm channel length, the profile of electric field of the wrapped FinFET channel has been simulated here. Along the y direction of the channel, the electric field profile has been studied and the profile has been shown in Fig. 6, FIg.7 and Fig.8. It has been observed from the simulation study that, the range of variation in the electric field along the y direction of the channel lowers with increasing the channel length and wrapped gate creates stronger electric field at the top of the channel.

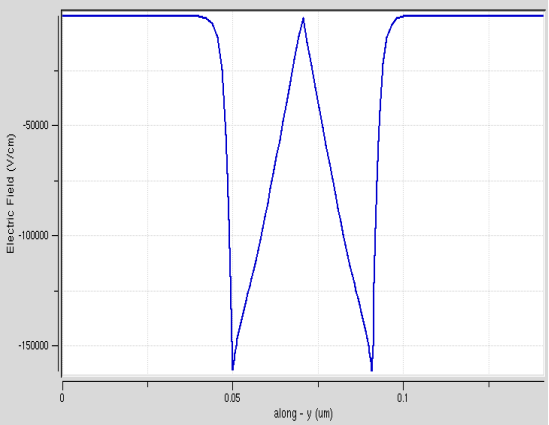

Fig. 6: Electric field profile for 40nm channel length

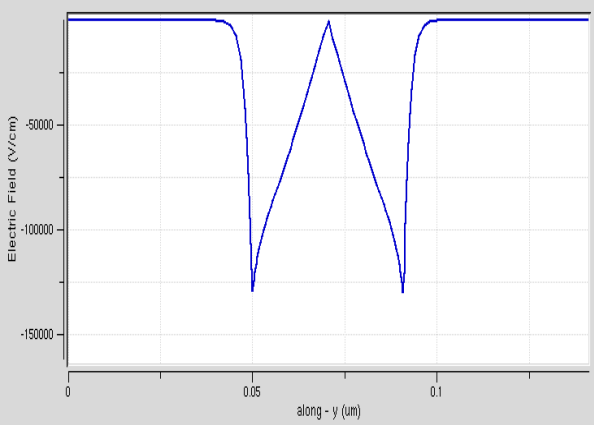

Fig. 7: Electric Field Profile for 50nm channel length

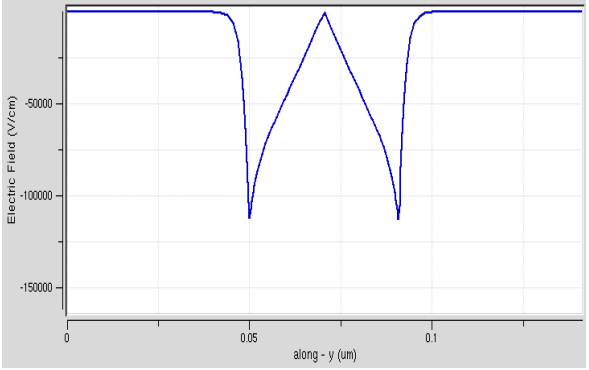

Fig. 8: Electric Field Profile for 60nm channel length

3.3 Electrostatic Potential along channel with varying channel length

Electrostatic potential along the FinFET channel has been simulated for three different values of channel length: 40nm, 50 nm and 60nm. The simulation curve has been shown in Fig.9. It has been observed from the simulation that, with increasing the channel length, electrostatic potential along the y direction of the channel increases significantly. For 40 nm channel length, around 0.30Volt electrostatic potential has been found in the simulation. For 60 nm channel length, the most minimum value of electrostatic potential has been seen in this figure. At around 0.070 nm channel length, most of the minimum value of electrostatic potential has been achieved.

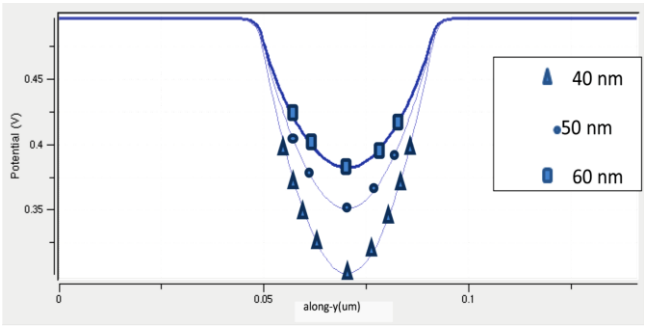

Fig. 9: Electrostatic Potential along channel for 40 nm, 50 nm and 60nm channel length

4. Results

In this simulation work, the electrical characteristics of double gate FinFET have been studied with varying the channel length of the wrapped channel of the FINFET device. Here, the drain current *VS* gate voltage characteristics, Electric field profile and electrostatic potential along the channel has been simulated for three different values of channel length: 40nm, 50 nm and 60nm. After studying and analyzing the simulation curves, it has been observed that, lowering the channel length, large amount of drain current can be obtained from the FinFET device for small gate voltage. From the electric field profile along the wrapped channel of FinFET it is seen that with decreasing the channel length, wide variation of electric field in the channel region of FinFET can be achieved which will be helpful to increase the mobility of carriers in the FinFE Tchannel and also it will decrease the electrostatic potential along the channel.

5. Conclusion

The electrical characteristics of double gate FinFET has been simulated in this research work with varying the channel length. The variation of drain current has been studied by varying the gate voltage for distinct values of channel length. Also the electrical field profile and electrostatic potential along the channel has been simulated for different channel lengths. In the result of this simulation based research, it has been suggested that lowering channel length will provide increased drain current, wide variation of channel electric field and decreased amount of

electrostatic potential along the wrapped channel of FinFET. In this research, we have investigated the variation of electrical characteristics of FinFET by changing the channel length and the results are shown in the plots. In future, the analysis of this simulation can be used to determine the electrical characteristics for trigate FinFET structure and it can also be applied for the fabrication purpose of highly electrically efficient FinFET [11].

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