

A Novel Fault Tolerant Reversible Gate and Its Application to Parity Preserving Adder Circuits

Noor Muhammed Nayeem, Lafifa Jamal and Hafiz Md. Hasan Babu

Department of Computer Science & Engineering, University of Dhaka, Dhaka, Bangladesh

noornayeem@gmail.com, lafifa@univdhaka.edu, hafizbabu@hotmail.com

Received on 14. 02. 2010. Accepted for publication on 19. 12. 2010

Abstract

This paper presents a novel reversible gate called Nayeem gate (NMG) which is parity preserving, that is, the parity of the outputs matches that of the inputs. One of the most widely used gates in reversible logic is Toffoli gate but it is not parity preserving. The most significant characteristic of NMG is that it can work singly as a parity preserving reversible Toffoli gate. The proposed gate can be used along with other existing parity preserving gates to synthesize circuits that detect a single error at primary outputs of a circuit. The applications of the proposed gate are demonstrated by realizing various types of adders such as full adder, ripple carry adder and carry skip adder. It has been shown that the proposed designs perform better than existing counterparts in terms of number of gates, number of garbage outputs, delay and quantum cost.

Keywords : Fault tolerant, Toffoli gate, adder, reversible logic

1. INTRODUCTION

Energy loss during computation is a very important issue in modern VLSI designs. Though the improvement in higher-level integration and the advancement of new fabrication processes have significantly reduced the heat loss over the last decades, there is a physical limit in the reduction of heat. Logic computation [1, 2] generates $kT \ln 2$ joules of heat energy for every bit of information loss where k is Boltzmann's constant and T is the absolute temperature of the environment. At room temperature the dissipating heat is around 2.9×10^{-21} J which is small but not negligible. Further, Bennett [3] showed that zero energy dissipation would be possible if the network consists of reversible gates only. The major application of reversible logic is in quantum computation as quantum circuits must be reversible [4]. Quantum computation is gaining popularity as some exponentially hard problems can be solved in polynomial time [5]. Reversible logic has also found its applications in several technologies, such as optical computing, ultra low power CMOS design and nanotechnology. Thus research in reversible logic is essential for the development of future technologies.

Reversible circuit is fundamentally different from traditional irreversible one as fan out is not allowed in reversible logic. Consequently, making a reversible circuit fault tolerant is much more complex than an irreversible logic circuit. Parity checking is one of the most widely used techniques for error detection in digital logic systems. If calculation is carried out in such a way that the parity of the input data is preserved

during the computation and, hence, at the output, intermediate checking is not necessary. Parhami [6] discussed the feasibility of the parity preserving approach in reversible logic circuits to detect single fault. This paper presents a novel fault tolerant gate called Nayeem gate (NMG) which is a new member in the family of parity preserving reversible gates. To synthesize reversible fault tolerant arithmetic logic unit, adders with fault toleration are very essential. This paper proposes an efficient approach to implement such adders which will play an important role in future fault tolerant quantum computers.

2. BASIC IDEAS OF REVERSIBLE LOGIC

This section describes basic definitions and ideas related to reversible logic along with the analysis of quantum cost.

Reversible Gate is a k -input, k -output (denoted by $k \times k$) circuit that produces a unique output pattern for each possible input pattern [7].

Let for any $k \times k$ reversible gate, the input vector be I_v , output vector O_v , and they are defined as follows, $I_v = (I_0, I_1, I_2 \dots I_{k-1}, I_k)$ and $O_v = (O_0, O_1, O_2 \dots O_{k-1}, O_k)$. There is a one to one correspondence between the vector of inputs and outputs, i.e., it can generate unique output vector from each input vector and vice versa. We denote this relationship as: $I_v \leftrightarrow O_v$.

Unwanted or unused output of a reversible gate (or circuit) is known as **Garbage Output**.

Feynman gate (FG) [8] is used to perform Exclusive-OR between two inputs. But in that case, one extra output will be generated as well, which is the garbage output as shown in Fig. 1 with *.

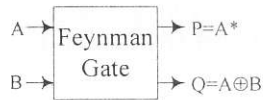


Fig. 1: Feynman Gate

Every reversible gate can be calculated in terms of quantum cost and hence the reversible circuits can be measured in terms of quantum cost. The *quantum cost* of every 2×2 gate is the same and the cost is unity [9, 10]. A 1×1 gate costs nothing and every quantum gate can be realized from 1×1 and 2×2 gates and its cost calculated as a total sum of 2×2 gates used [9].

The quantum cost of FG is 1 and the quantum cost of Feynman Double Gate (F2G) [6] is 2.

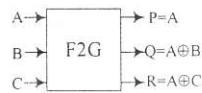


Fig. 2: Feynman double-gate (F2G)

Parity Preserving Reversible Gate is a reversible gate for which the parity of the outputs is equal to that of the inputs [6]. In other words, input parity is preserved at the output bits. As the reversible gates have the same number of inputs and outputs, a sufficient condition for designing parity preserving reversible circuits with such gates is that each gate must be parity preserving [6]. Fredkin Gate (FRG) [11] of Fig. 3 and Feynman Double Gate (F2G) of Fig. 2 are parity preserving reversible gates because each of these two gates satisfies the relation $A \oplus B \oplus C = P \oplus Q \oplus R$. It is to be noted that well known Toffoli Gate (TG) [12] of Fig. 4 is not parity preserving, it can be proved by comparing the input parity ($A \oplus B \oplus C$) to the output parity ($P \oplus Q \oplus R$).

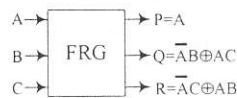


Fig. 3: Fredkin gate (FRG)

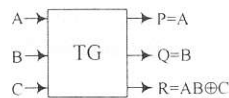


Fig. 4: Toffoli gate (TG)

3. Proposed 4×4 Parity Preserving Reversible Gate

This paper proposes a 4×4 reversible gate called Nayeem gate (NMG) which is shown in Fig. 5. This gate is defined as $I_v = (A, B, C, D)$ and $O_v = (P=A, Q=B \oplus D, R=\overline{AD} \oplus AB, S=\overline{AD} \oplus AB \oplus C)$, where I_v and O_v are the input and output vectors respectively. The corresponding truth table of the gate is shown in Table I. It is obvious from the truth table

that the input pattern corresponding to a particular output pattern can be uniquely determined. It can be verified from the truth table that the outputs preserve the input parity. In other words, NMG satisfies the relation $A \oplus B \oplus C = P \oplus Q \oplus R$. Quantum equivalent representation of NMG is shown in Fig. 6. Its quantum cost is 7.

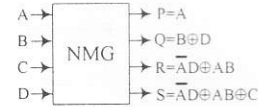
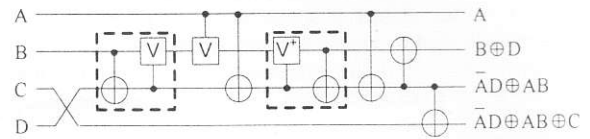
Fig. 5: Proposed reversible 4×4 Nayeem gate (NMG)

Fig. 6: Quantum equivalent realization of Nayeem gate (NMG)

Table 1: Truth table of the proposed Nayeem gate

Inputs				Outputs			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	0	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	1	0	0
1	0	1	0	1	0	0	1
1	0	1	1	1	1	0	1
1	1	0	0	1	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	1	0	1	0

4. Applications of the Proposed NMG

This section describes the applications of the proposed NMG. NMG can be used to synthesize parity preserving TG, full adder, ripple carry adder and carry skip adder. It has been shown that the proposed fault tolerant circuits designed using the proposed gate are the most optimized one compared to their existing counterparts in literature.

A. Synthesis of Parity Preserving Toffoli Gate (TG)

TG is not parity preserving. One of the important functionality of the proposed Nayeem gate is that that it can work singly as a parity preserving TG. Fig. 7 shows the implementation of the proposed gate as the parity preserving TG.



Fig. 7: Proposed NMG working singly as parity preserving TG

Optimality of the proposed parity preserving TG can be easily understood from Table 2 which shows the comparative study with the existing counterparts.

Table 2: Comparison of different parity preserving TG circuits

	No. of gates	Garbage Output	Unit Delay	Quantum Cost
Existing Circuit [10]	3	2	3	9
Existing Circuit [18]	2	1	2	7
Proposed Circuit (Fig. 7)	1	1	1	7

B. Synthesis of Parity Preserving Reversible Full Adder

A full adder is a circuit that performs an addition operation on three bits (A, B and C_{in}) and produces two outputs: a sum bit ($S = A \oplus B \oplus C_{in}$) and a carry bit ($C_{out} = A.B \oplus B.C_{in} \oplus A.C_{in}$). A parity preserving full adder circuit was proposed by Haghparast *et. al.* [13]. The design [13] requires 6 reversible gates, produces 6 garbage outputs, needs 18 quantum cost, and delay is 6. Proposed Nayeem gate has also its application in realizing efficient parity preserving reversible full adder. Fig. 8 shows the proposed full adder circuit with the help of NMG and F2G gates. The proposed design uses only parity preserving gates, hence the adder is parity preserving.

Table 3 shows the comparative analysis of the proposed parity preserving reversible full adder with the existing circuits.

C. Synthesis of Parity Preserving Reversible Ripple Carry Adder

A ripple carry adder is built using full adders connected in cascade, with the output carry from each full adder linked to the input carry of the next full adder in the chain. Using proposed full adders, Fig. 9 presents an n -bit ripple carry adder which is parity preserving. It requires n parity

preserving full adder circuits, thus it can realized by $4n$ gates, $6n$ garbage outputs with quantum cost of $18n$.

Table 3: Comparison of different parity preserving reversible full adders

	No. of gates	Garbage Output	Unit Delay	Quantum Cost
Existing Circuit [18]	6	6	6	18
Proposed Circuit (Fig. 8)	4	6	4	18

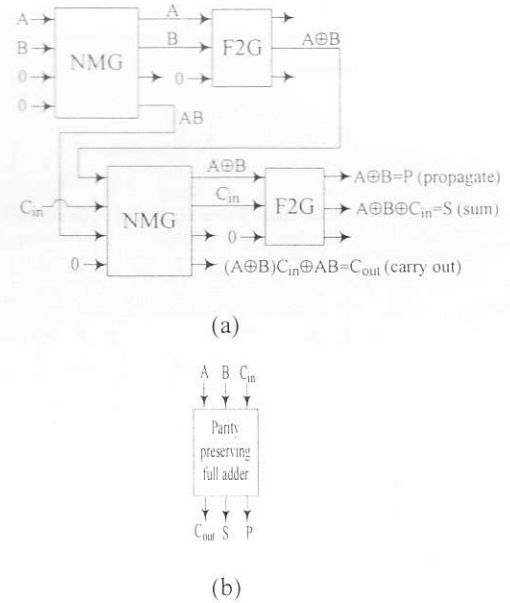


Fig. 8: Proposed parity preserving reversible full adder: (a) structure; (b) block diagram

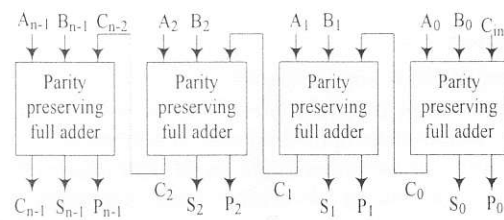


Fig. 9: Proposed parity preserving reversible ripple carry adder

D. Synthesis of Parity Preserving Reversible Carry Skip Adder

Carry skip adder is typically divided into m -bit blocks. It looks for cases in which carry-out of a block is equal to carry-in. Let, C_{in} and C_{out} be carry-in and carry-out of a block respectively. Again let, A_i and B_i be the inputs to i^{th} stage (full adder). Propagation $P_i = A_i \oplus B_i$. If either A_i or B_i is 1, then P_i will be 1. If all P_i in a block are 1, then block propagation, P_B is 1. $P_B = 1$ allows C_{in} to “skip” m stages within block and generates C_{out} . Thus if P_B is 1, C_{in} will be propagated to the C_{out} . However, in the other case, C_{out} will be generated in the ripple carry fashion.

Fig. 10 shows the proposed parity preserving reversible carry skip adder. The F2G is used to avoid fan out and to produce two copies of block carry-in (C_{in}). Each of the four full adder circuits computes propagation (P_i), sum (S_i) and stage carry (C_i). The middle three FRGs compute $P_B = P_0 \times P_1 \times P_2 \times P_3$. As FRG is a controlled swap gate, if $P = 1$ then bottom FRG selects $C_{out} = C_{in}$ which is independent of C_3 , otherwise, C_{out} will be C_3 . It requires 21 gates, produces 29 garbage outputs and needs 40 quantum cost.

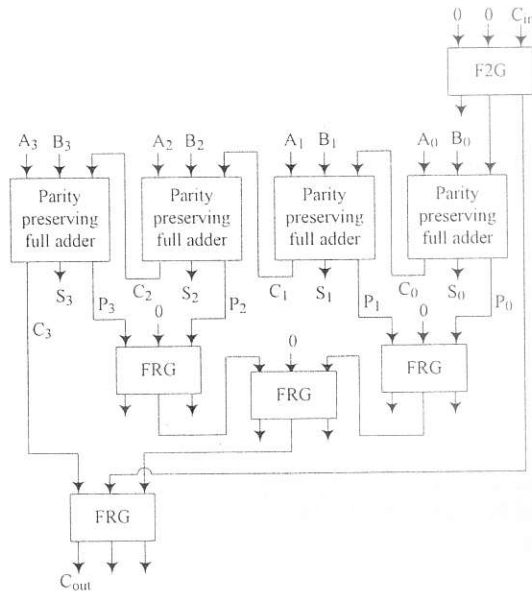


Fig. 10: Proposed parity preserving reversible 4-bit carry skip adder block

5. Conclusion

The renowned TG is not parity preserving. Thus it can not be used in the design of parity preserving reversible circuits. This paper proposed an optimized way to synthesize TG with parity preservation by presenting a novel fault tolerant NMG gate. Parity preserving reversible logic syntheses were carried out for full adder, ripple carry adder and carry skip adder using the proposed gate. Efficiency of the proposed designs was clearly highlighted by means of comparison tables which prove that the new designs are clearly better than the existing one. In a nutshell, applications of TG can be replaced by NMG in parity preserving reversible logic. This

approach provides a way of incorporating fault tolerance into reversible circuits without much extra design effort and with modest hardware overhead. This research forms an important step in the building of complex reversible fault tolerant circuits for quantum computers. In future, we have the target to find some other applications of the proposed gate as well as the simulation results of the circuits using benchmark functions.

References

1. R. Keyes and R. Landauer, "Minimal energy dissipation in logic," IBM Journal of Research and Development, vol. 14, pp. 152-157, 1970.
2. R. Landauer, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 5, pp. 183-191, 1961.
3. C. H. Bennett, "Logical reversibility of computation," IBM Journal of Research and Development, vol. 17, no. 6, pp. 525-532, 1973.
4. M. Nielsen and I. Chuang, Quantum Computation and Quantum Information, Cambridge Univ. Press, 2000.
5. V. V. Shende, A. K. Prasad, I. L. Markov, and J. P. Hayes, "Synthesis of reversible logic circuits," IEEE Transactions on CAD, vol. 22, no. 6, pp. 710-722, June 2003.
6. B. Parhami, "Fault Tolerant Reversible Circuits," Proceedings of 40th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, October 2006, pp: 1726-1729.
7. H. M. H. Babu, M. R. Islam, S. M. A. Chowdhury, and A. R. Chowdhury, "Synthesis of Full-adder Circuit Using Reversible Logic," Proceedings of 17th International Conference on VLSI Design (VLSI Design 2004), Mumbai, India, January 2004, pp.757-760.
8. R. Feynman, "Quantum mechanical computers," Foundations of Physics, vol. 16, no. 6, pp. 507-531, 1986.
9. M. Perkowski et al., "A Hierarchical Approach to Computer-aided Design of Quantum Circuits," Proceedings of 6th International Symposium on Representations and Methodology of Future Computing Technology, RM 2003, Trier, Germany, March 10-11, pp. 201-209.
10. J. Smoline and D. P. DiVincenzo, "Five two-qubit gates are sufficient to implement the quantum Fredkin gate," Physical Review A, vol. 53, no. 4, pp. 2855-2856, 1996.
11. E. Fredkin and T. Toffoli, "Conservative logic," International Journal of Theoretical Physics, vol. 21, pp. 219-253, 1982.
12. T. Toffoli, "Reversible Computing," Tech memo MIT/LCS/TM-151, MIT Lab for Comp. Sci, 1980.
13. M. Haghparast and K. Navi, "Design of a novel fault tolerant reversible full adder for nanotechnology based systems," World Applied Sciences Journal, vol. 3, no. 1, pp. 114-118, 2008.