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A Novel Approach to Design Ternary Reversible Barrel Shifter

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Abstract

Ternary logic synthesis methods have recently been introduced to realize multi-input ternary logic functions using cascades of ternary permutative gates. Design of Ternary Reversible Barrel Shifter is first proposed in this paper. The proposed design methodology is based on first realizing the circuit using Ternary Feynman gates and Ternary Modified Fredkin Gate (MFG). Then we have analyzed the performance of the proposed circuit mathematically to define lower bounds for the number of the basic gates, garbage outputs and ancilla bits.

Keywords : Reversible Logic, Ternary System, Regards, Ahsan

1. Introduction

According to Landauer [1], binary logic circuits built using traditional irreversible gates lead certainly to energy dissipation. Landauer and Bennett [1, 2] proved that losing information in a circuit causes losing power. The gate that does not loose information and has a one-to-one mapping between the input values and the output values is called reversible. At present, Quantum computing is one of the most emerging research fields which is absolutely reversible and may lead to zero power dissipation. Among different multiple-valued quantum logics, ternary quantum logic is the most prominent one. Muthukrishnan and Stroud [3] showed realization of d-valued ($d > 2$) quantum gates using liquid ion-trap. Synthesis techniques of ternary reversible quantum adder subtractor, encoder and decoder, multiplexer and demultiplexer are proposed recently in [4-6].

In this paper, we propose reversible realization of a ternary barrel shifter using macro-level ternary Feynman and Modified Fredkin Gates (MFG). Though, binary reversible barrel shifter has been proposed recently [7], but the ternary reversible barrel shifter is first ever proposed in this paper.

Rest of the paper is organized as follows: Section 2 provides the necessary background study on ternary quantum logic with ternary reversible logic gates. Reversible binary barrel shifter is presented in Section 3. Design of Ternary Barrel Shifter is proposed in Section 4. Section 5 gives performance evolution of the propounded circuits using different parameters. Finally, Section 6 draws conclusion of the paper.

2. Ternary Logic and Ternary Gates

This section presents the necessary background and preliminaries in order to help the reader to comprehend the newly proposed architecture that will be presented in Section 4.

2.1. Ternary Logic

A ternary, three-valued or trivalent logic or 3VL is a generalization of multi-valued logic with three truth values indicating true, false and neither true nor false [10]. To define a ternary reversible circuit, let $B = \{0, 1, 2\}$, where B is a three valued vector. A ternary logic circuit f with n input variables $B_1,\ldots,B_n$, and n output variables, $Q_1,\ldots,Q_n$, is denoted by $f : B^n \rightarrow B^n$, where $\langle B_1,\ldots,B_n\rangle \in B^n$ is the input vector and $\langle Q_1,\ldots,Q_n\rangle \in B^n$ is the output vector. A ternary logic circuit is reversible if it has one-to-one and onto (bijection) mapping between inputs and outputs [10].

Ternary logic values of 0, 1, and 2 are represented by a set of distinguishable different states of a qutrit (quantum ternary digit), which can be a photon's polarizations or an elementary particle's spins. Qutrit states are represented by $|0\rangle$, $|1\rangle$ and $|2\rangle$ [4]. Ternary logic includes Ternary Galois Field (TGF) operations: addition and multiplication and they are basically modulo 3 operations [11].

2.2 Ancilla Bit and Garbage Output

An Ancilla bit [9] is an auxiliary input constant bit needed in the circuit other than the function input bits. On the other hand, Garbage Outputs are the bits of a Reversible Gate (or Reversible Circuit) that are not used as output or input to any other gate (or circuit). Garbage Outputs are required only to remain the one-to-one mapping between input and output vector. Both the terminologies play very important role in Reversible Synthesis as they are considered as two prime parameters of reversible circuit minimization.

2.3 Ternary Feynman Gate

A 2*2 ternary Feynman gate is shown in **Fig. 1**. Here A is the controlling input and B is the controlled input. The output P is equal to the input A and the output Q is GF3 sum of A and B. If $B = 0$, then $Q = A$, then the ternary Feynman gate acts as a copying gate [11]. Galois Field 3 (GF3) consists of the set of elements $T = \{0, 1, 2\}$ and two basic binary operations – addition and multiplication. Readers

should note that GF3 operations are nothing but modulo 3 operations [4].

2.4 Modified Fredkin Gate (MFG)

Fredkin Gate (FG) is the fundamental concept in reversible and quantum computing [12]. Fredkin gate is a binary gate, and MVL counterpart of this gate was introduced in [13], which is called by Modified Fredkin Gate (MFG). Multi-value logic (MVL) is defined as a non-binary logic and involves the switching between more than 2 states. We will assume that multi-value logic devices will be limited to 2 inputs/single output functions. A ternary or 3-value logic function is one that has two inputs which can assume three states (say 0, 1 and 2) and generates one output signal that can have one of these three states [15]. **Fig. 2** shows the block diagram of Modified Fredkin Gate (MFG).

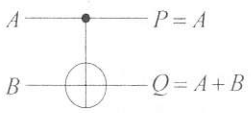

Fig. 1. Modified Fredkin Gate [13

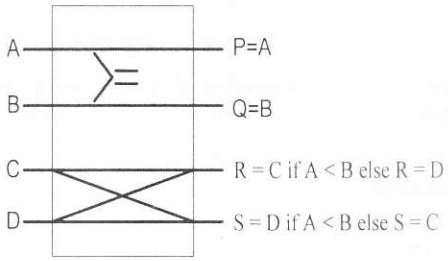

Fig. 2: 2*2 ternary Feynman gate [11]

2.5 Barrel Shifter

A barrel shifter is a combinational logic circuit, which receives an n-bit input data, k-bit, shift value and will produce an n-bit shifted result, (n, k) barrel shifter). Barrel shifters can perform multi-bit shifts in a single cycle [7]. There are two architectural layouts for shifters - array shifters and logarithmic shifters [14]. A logarithmic shifter with n-bit data value is divided into $\log_2 n$ stages. Each bit of the shift value is sent to a different stage of the shifter. Each stage handles a single, power-of-two shift. The input data will be shifted or not shifted by each of the stages [14].

3. Binary Reversible Barrel Shifter

In this section we discuss about the reversible design of a binary barrel shifter [7, 9], as the design in [9] is the most recent one, we will show the diagram of that design. Feynman and Fredkin gates are used in order to produce fan-outs. According to this design, reversible (4, 2) barrel shifter [9] requires 6 Fredkin gates and Feynman Gates, but most importantly, the design works only with binary inputs (shown in Fig. 3).

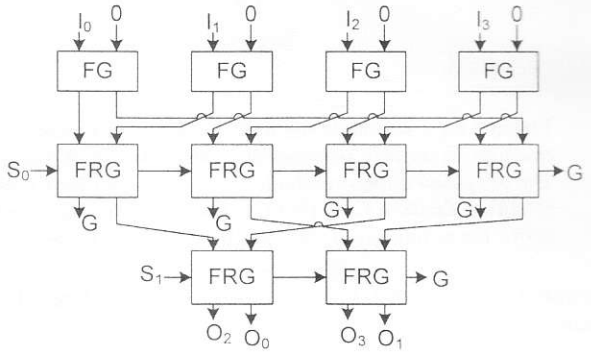

Fig. 3: Existing reversible (4, 2) barrel shifter [9]

4. Ternary Reversible Barrel Shifter: The Proposed Architecture

In order to develop the proposed design, we have closely examined the architecture and work flow of the existing binary one [7]. A traditional barrel shifter with k-bit shift value uses 2^k copies of each input data. We are considering an example of a Ternary (4, 2) Reversible Barrel Shifter to comprehend the idea clearly. The proposed circuit contains Feynman gates in order to produce 2^k copies of each input data to act as inputs for the next level, as shown in Fig. 4. We have used constant 0 and 1 for left shift and right shift, respectively.

The next stage consists of two stages of MFGs for shifting operation. First stage of ternary barrel shifter with MFGs is shown in Fig. 5. Ternary MFG is a four input gate (Fig. 2). The constant select input acts as input A, the two inputs from the upper layer act as B and C. Now the last input D is provided by constant input 0 and for this purpose we need four more Feynman gates. The outputs from the first level are propagated to the next stage. In the second stage, we use four MFGs (Fig. 6) to produce the desired shifted result. The outputs from the upper stage are connected to a layer of four MFGs to get a unique data output pin, regardless of shifting direction left/right (Fig. 7). We provided constant inputs to the final level of MFGs. For right shift constant (0, 1) combination is used as the first two inputs, for left shift it is otherwise. So, the final and complete architecture of ternary reversible (4, 2) barrel shifter with four bits as data value and 2-bit shift value is depicted in Fig. 8. Next we show a general structure of (n, k) ternary barrel shifter in Fig. 9.

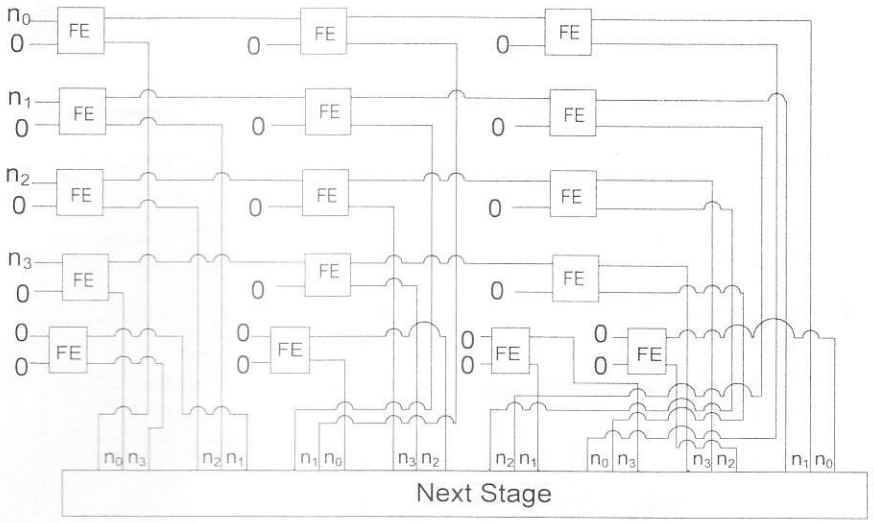

Fig. 4: Feynman gates to copy inputs

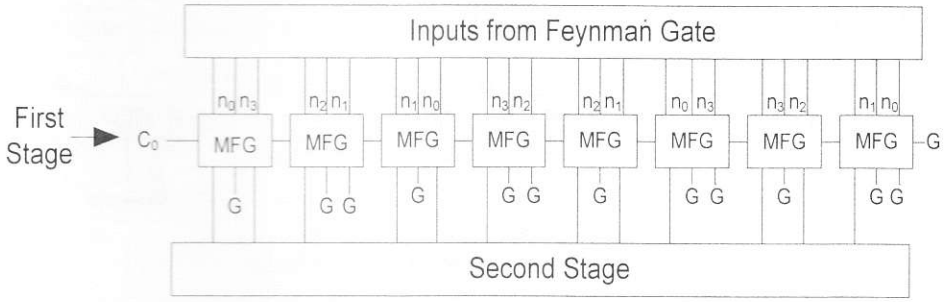

Fig. 5: First stage of ternary barrel shifter

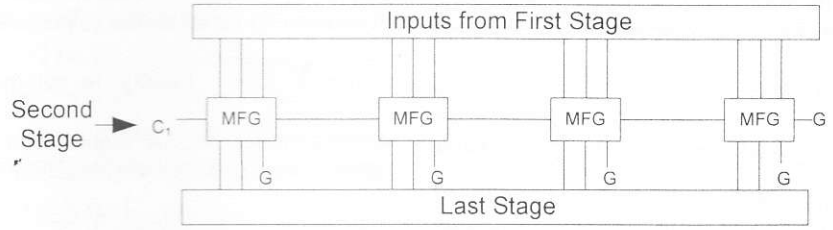

Fig. 6: Second stage of ternary barrel shifter

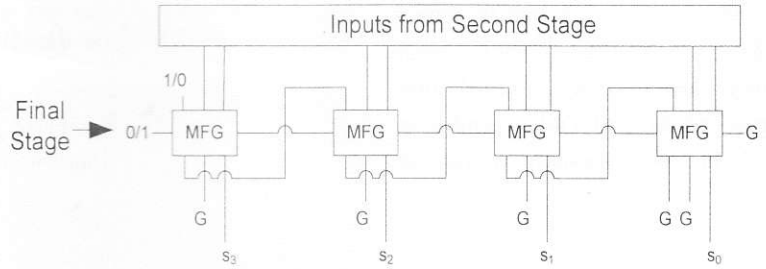

Fig. 7: Final stage of ternary barrel shifter

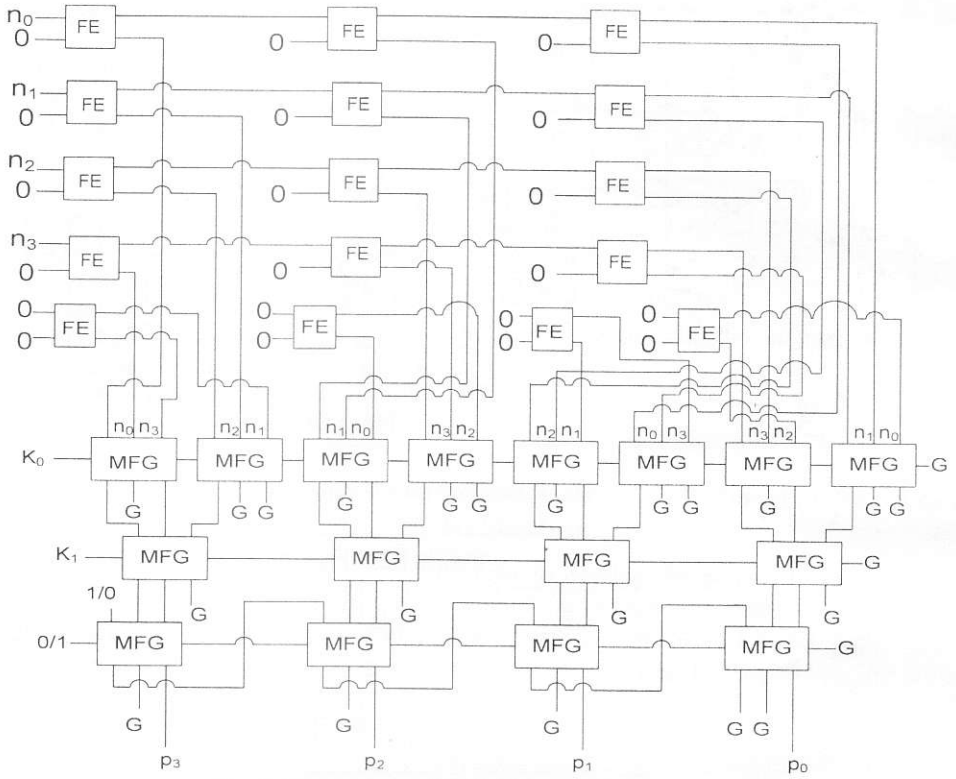

Fig. 8: Ternary Reversible (4, 2) Barrel Shifter

5. Performance Evaluation

In this paper, we have deduced several equations to anticipate the lower bounds of the basic gates, garbage bits and ancilla bits [9] for estimating the performance of the proposed circuit. Inductive proofs of these equations are given below.

Theorem 5.1: *A Ternary Reversible (n, k) Barrel Shifter can be realized with at least* $n\times\left(2^k+k-1\right)+n\times\sum_{i=1}^{k}2^{k-i}$ *gates, where n is data value and k is shift amount.*

Proof: Theoretically, each bit of the operand should be copied 2^k times for their future usage, but can avoid single gate, as we can use both outputs of the last column of Feynman Gates. This copy is required for every n bit, and hence, total number of Feynman gates required to copy n bits is $n\times\left(2^k-1\right)$. For generating Constant input 0, (which can be avoided using individual 0's), we required more $n\times(k-1)$ Feynman Gates. As a result, total number of Feynman gates required in the proposed design is: $n\times\left(2^k-1\right)+n\times(k-1)$. For performing shifting operations, we require k levels of MFGs. For each i^{th} level $(1\le i\le k)$, we require $n\times 2^{k-i}$ MFGs. So, total number of MFGs for a ternary (n, k) barrel shifter to perform bit shifting operations is $n\times\sum_{i=1}^{k}2^{k-i}$. Finally, to get the output of the shifter from a unique pin, we require n more MFGs. As a result, total number of MFGs required in the proposed design is:

$$n\times\sum_{i=1}^{k}2^{k-i}+n.$$

Hence, the total number of gates to build the proposed circuit is:

$$n\times\left(2^k-1\right)+n\times(k-1)+n\times\sum_{i=1}^{k}2^{k-i}+n$$

$$=n\times\left(2^k+k-1\right)+n\times\sum_{i=1}^{k}2^{k-i}$$

■

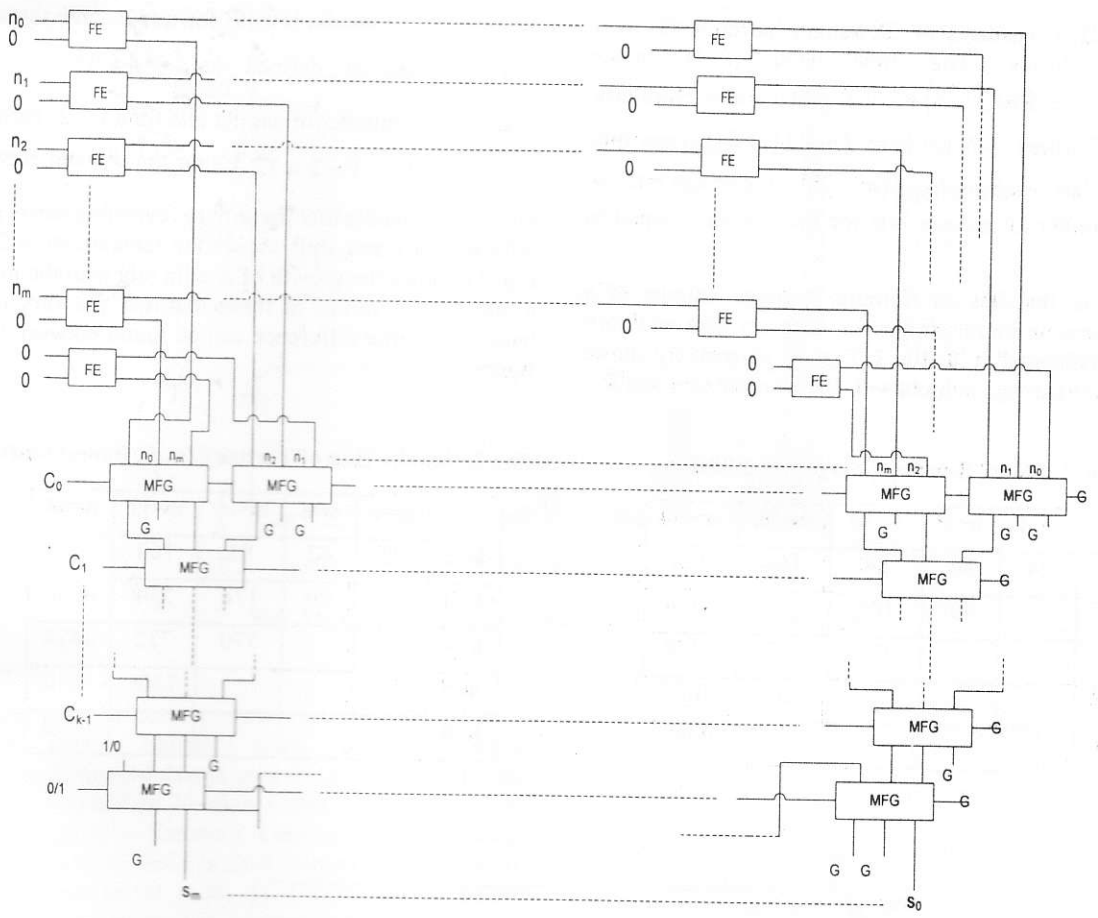

Fig. 9: Ternary Reversible (n, k) Barrel Shifter

Example 5.1: Consider a (4, 2) ternary barrel shifter. In this case, the number of Feynman Gates is $n \times (2^k - 1) = 4 \times (2^2 - 1) = 12$. For generating constant input 0, we require $n \times (k-1) = 4 \times (2-1) = 4$ Feynman Gates which sums up the number of Feynman Gates to 16. For performing shifting operation, we require $n \times \sum_{i=1}^{k} 2^{k-i} = 4 \times [2^{2-1} + 2^{2-2}] = 12$ MFGs and to get the output from a unique pin, we further require 4 more MFGs. So, in total, we need 16 MFGs (**Fig. 8**).

Theorem 5.2: *Let T_{GO} be the total number of garbage outputs produced by a Ternary Reversible (n, k) Barrel Shifter, then* $T_{GO} = n\left[\sum_{i=1}^{k-1} 3 \times 2^{k-(i+1)}\right] + 2(n+1) + k$, *where n is data value and k is shift amount.*

Proof: In a ternary reversible (n, k) barrel shifter, we have k levels of MFGs. For each i^{th} level $(1 \le i \le (k-1))$, we get $n(3 \times 2^{k-(i+1)}) + 1$ garbage bits. For i^{th} level, where $i=k$, we have $(n+1)$ garbage outputs. Finally, for the last level of MFGs, which is used for getting a unique output pin, we have $(n+2)$ number of garbage bits. Therefore, the total number of garbage bits produced by a (n, k) barrel shifter is:

$$T_{GO} = n\left[\sum_{i=1}^{k-1} 3 \times 2^{k-(i+1)}\right] + (k-1) + (n+1) + (n+2)$$

$$= n\left[\sum_{i=1}^{k-1} 3 \times 2^{k-(i+1)}\right] + k + 2n + 2$$

$$= n\left[\sum_{i=1}^{k-1} 3 \times 2^{k-(i+1)}\right] + 2(n+1) + k \quad \blacksquare$$

Example 5.2: Consider a (4, 2) ternary barrel shifter with two shift levels. The first level ($i=1$) makes $n\left(3\times 2^{k-(i+1)}\right)+1=4\left(3\times 2^{2-(1+1)}\right)+1=13$ garbage bits. Similarly, for i^{th} level, where $i=2$, we have $(n+1)=5$ garbage bits. Finally, the last level produces $(n+2)=6$ garbage bits. So the total number of garbage bits for this circuit is equal to 24(**Fig. 8**).

According to the derived formula, garbage outputs of a ternary reversible barrel shifter for different data and shift values are tabulated in **Table. 1**. Fig. 10 extensively shows the growth of garbage outputs with the increase of n and k.

The number of ancilla bits [9] for a reversible ternary (n, k) barrel shifter, is defined as: $\frac{3}{2}\times n\times 2^{k}-n+2$. For example, the number of ancilla bits for a (4, 2) barrel shifter is: $\frac{3}{2}\times 4\times 2^{2}-4+2=22$ .Using the derived formula, the numbers of ancilla bits for ternary reversible barrel shifter of different data and shift values are tabularized in **Table. 2**. Fig. 11 shows the growth of ancilla bits with the increase of n and k. The values of these matrices are very close and hence very little difference can be found between these two figures.

Table 1: GO of Ternary (n, k) Barrel Shifter

	n=4	n=8	n=16	n=32	n=64
k=2	24	44	84	164	324
k=3		93	181	357	709
k=4			374	742	1478
k=5				1511	3015
k=6					6088

Table 2: Ancilla Bits of Ternary (n, k) Barrel Shifter

	n=4	n=8	n=16	n=32	n=64
k=2	22	42	82	162	322
k=3		90	178	354	706
k=4			370	732	1474
k=5				1506	3010
k=6					6082

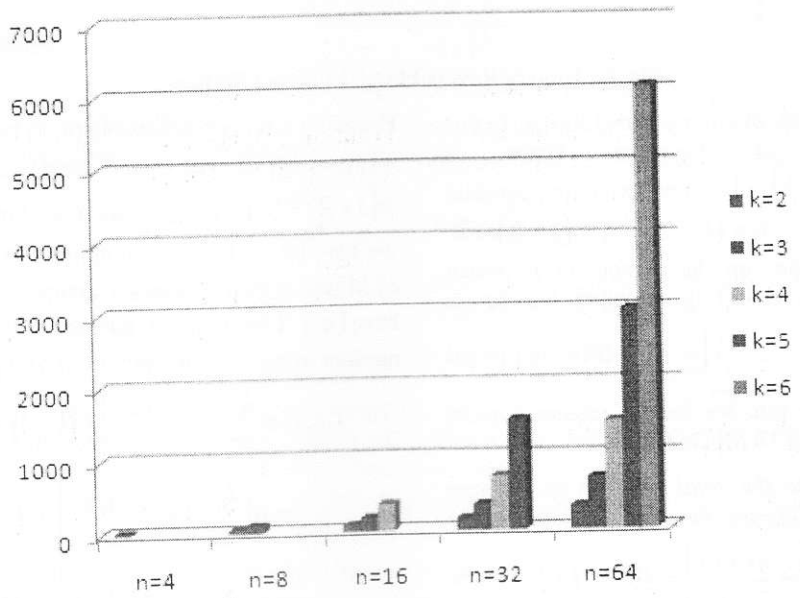

Fig. 10: Garbage outputs for different n and k values

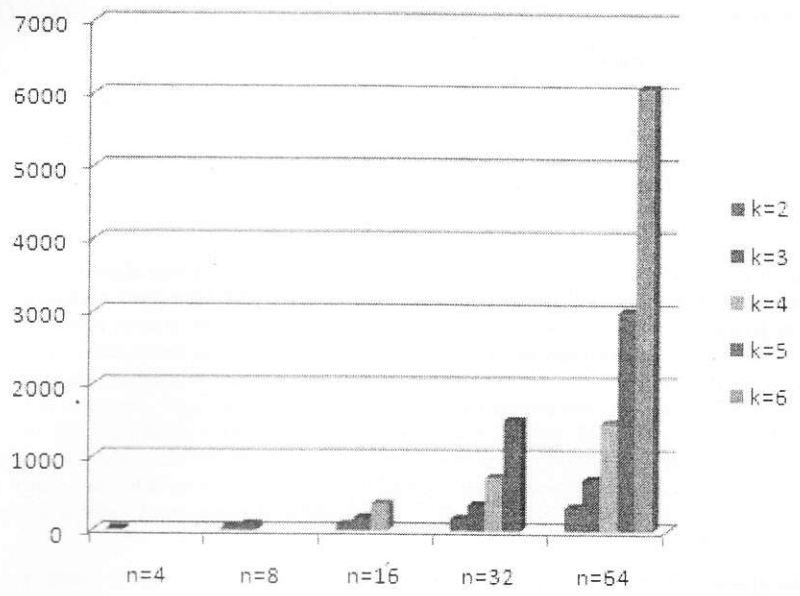

Fig. 11: Growth of Ancilla Bits for Different n and k values

6. Conclusion

This paper introduces a new architecture: Ternary Reversible Barrel Shifter, along with its design methodology. Proposed design uses the macro-level Ternary Feynman and Modified Fredkin Gates, which are widely used Ternary gates in literature. Generalized (n, k) design, where n is data value and k is shift amount, is shown with a step by step design of a (4, 2) Ternary Barrel Shifter. Finally, we have evaluated the proposed circuit in terms of various n and k values. Future research includes equivalent realization of the propounded circuit using M-S gates.

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