

Proposition of a Multipurpose Quantum Gate Capable of Computing All Elementary 1-bit and 2-bit Logical Operations

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Abstract

This paper presents a 3-Qubit quantum gate which is capable of computing all elementary 1-bit and 2-bit logical operations. The contribution of this work is in the section of obtaining classical computation via quantum principle. The proposed gate is intended to eliminate the impacts of ancillary/ garbage outputs which are introduced basically due to the limitations of implementing classical irreversible logic using reversible quantum gates. The methodology used in this purpose is dynamically changing the control and target qubits for different computational purpose. With a number of truth tables, block diagrams and logical analysis it is shown that, this gate performs classical 1-bit SET, RESET, FLIP, NULL and 2-bit AND, OR, XOR, NAND, NOR, XNOR operations with some additional properties such as level-2 FAN-OUT, Universality etc. Since, gate minimization is one of the bigger challenges in quantum computation, it is anticipated that, introduction to such a gate can reduce bulks of algorithm complexity as well as explore some new dimensions of applicability.

Keywords : Quantum Computation, Quantum Gate, Multipurpose Quantum Gate

1. Introduction

A quantum computer is a device for computation that makes direct use of quantum mechanical phenomena, such as superposition, entanglement, to perform operations on data. Quantum computation has received considerable attention in recent years especially at the bottom line of the semiconductor age. Basically, Quantum physics is the most accurate science known this far, to describe or analyze the universe (or may be multiverse) around us; and the product of this discipline in the field of computation is believed (and also verified in many cases) to be the most powerful and efficient among all existing or upcoming technologies. In some sense, it can be said that, quantum computation is the most natural way of computation. Though it is believed to be incredibly fast, unbelievably small and extremely durable technology at its matured age, this is not all of it; Quantum computation introduces completely new concepts of computation, which can change the definition of the technology we have today.

Although quantum computing is still in its infancy, experiments have been carried out in which quantum computational operations were executed on a very small number of qubits. Both practical and theoretical research continues with interest, and many national government and military funding agencies support quantum computing research to develop quantum computers for both civilian and national security purposes, such as cryptanalysis [1].

This paper work is entirely theoretical and not oriented with the new concept of computations introduced by quantum

physics. The objective of this work is obtaining classical binary computations by means of quantum principle in an efficient way; and in this purpose, a 3-qubit gate is proposed. In the following sections, the proposed gate is elaborately shown, analyzed and the potential abilities of this or this kind of gates are discussed.

2. Background of the work

It is possible to simulate a classical logic circuit using a quantum circuit. It would be very surprising if this were not the case, as physicists believe that all aspects of the world around us, including classical logic circuits, can ultimately be explained using quantum mechanics. But, this can't be done directly as because unitary quantum logic gates are inherently reversible, whereas many classical logic gates such as the AND, OR, NAND, NOR gate are irreversible. For example logical AND is basically a gate which maps several input bits to one output bit with the logical operation that *the output will be 0 if any of the inputs are 0*. Hence, for such an irreversible 2-bit operation, by any means it is not possible to design a 2-qubit gate which performs the exact same logic [2]. Moreover there are some properties of a quantum gate which arise difficulties to implement classical operations, such as quantum gates do not support FAN-IN and FAN-OUT, and they are Acyclic [3, 4, 5].

A very much popular gate especially in this context is **Toffoli** gate introduced by Tommaso Toffoli in 1980. This is a 3-qubit gate in quantum logic; the functional name of this gate is CCNOT (Controlled Controlled NOT operation) gate. In order to explain the motivation of this work, the basics of the Toffoli gate is shown in Fig.1.

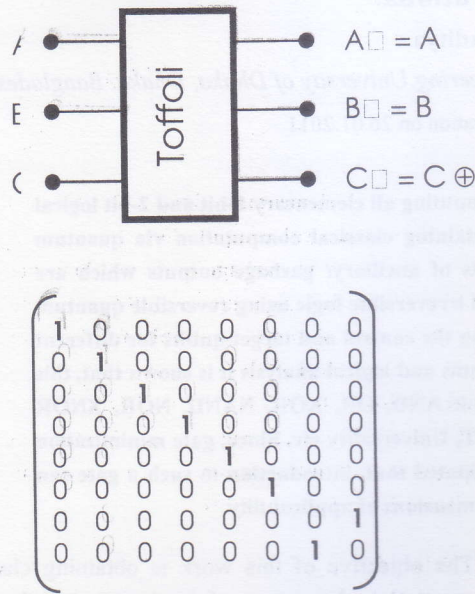


Fig. 1: Block diagram and 8 X 8 Matrix representation of Toffoli gate

The reason of calling this CCNOT gate is, if the inputs A and B both are set to logical 1 state, the output C' will be the inverted of corresponding input C. Two important properties of this gate are shown in Fig.2.

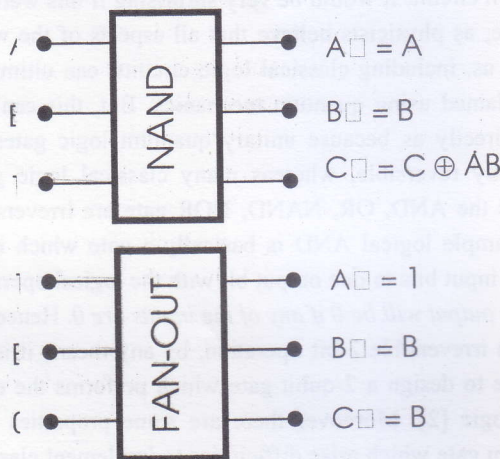


Fig. 2: Block diagram and 8 X 8 Matrix representation of Toffoli gate

As the NAND gate is a Universal gate in the context of classical computation, together with these two properties, any classical circuit can be simulated by an equivalent reversible circuit [6]. Hence, Toffoli gate is the principle

gateway and it ensures that quantum computers are capable of performing any computation which a classical (deterministic) computer may do.

Now, let's consider representation of the Toffoli gate shown in Fig.3 which serves as a classical AND gate.

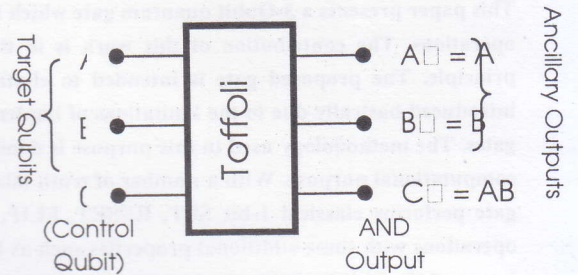


Fig. 3: Toffoli gate in Logical AND mode operation

As shown here, the input control Qubit C is the set to 0 in order to achieve the AND operation of input A and B at output C'. But, what do the outputs A' and B' do? These simply follow their corresponding inputs and do not contribute anything to the target operation. These are the Ancillary or Garbage outputs, the cost of preparing irreversible logics with reversible circuits [7]. These unwanted outputs not only reduce the overall efficiency, but also increase the complexity in algorithm and circuit designing.

But, it is also a fact that, it must have to be at least a 3-qubit system to simulate a 2-bit AND or any irreversible operation. Since, a 3-qubit gate is much more capable than computing simply a few 2-bit operations, in this work a standalone quantum gate is proposed and carefully designed which is meant to do all elementary 1-bit and 2-bit classical operations. The problems with the ancillary outputs are strategically reduced using dynamic control inputs. Therefore, obviously it is expected that, such a multipurpose quantum gate will offer a better gateway between classical and quantum computers. The fundamental property that this proposed gate shows is a kind of Parallel Universality for 1-bit and 2-bit operations and from now on, this gate will be shortly denoted as PU gate in the following sections.

3. Design Considerations

As stated earlier, PU is a 3-qubit gate which is designed to perform the operations elaborated in Fig.4.

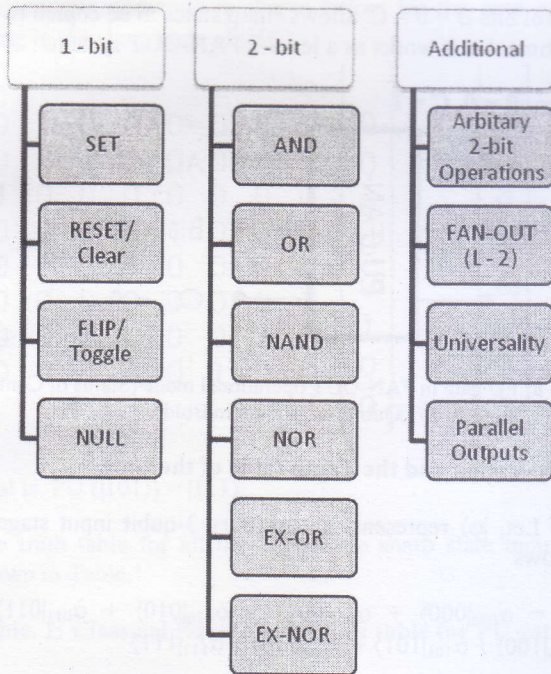


Fig.4: Functionalities and Design issues of PU gate

4. Matrix for the PU gate

The most convenient way of representing a quantum gate is by means of a Unitary Matrix. Here, the matrix representation for the designed PU gate is illustrated in Fig.5.

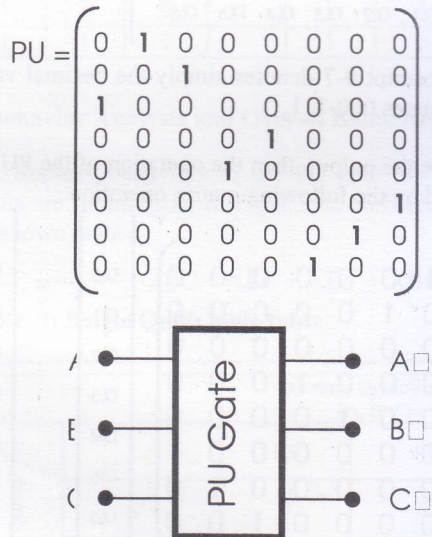


Fig. 5: Infrastructure of PU gate (a) Standard 8 X 8 matrix representation (b) Basic Block Realization

According to the theory of quantum gates, any arbitrary n-bit quantum gate can be represented by a $2^n \times 2^n$ Unitary

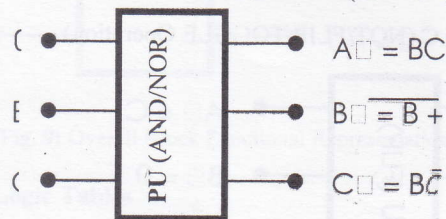
matrix and the vice versa [3]. Here the matrix for PU gate is an 8 X 8 unitary matrix and therefore represents a valid 3-Qubit quantum gate. A basic block is also shown in the figure above in order to explain the properties/ features in the section 5.

5. Functionalities of the gate

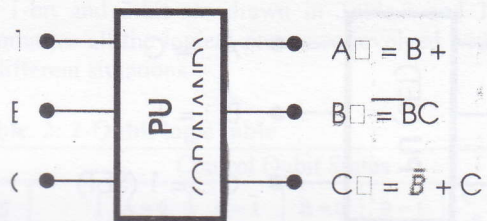
The gate is designed to use 1 control Qubit for the 2-bit operations and 2 control Qubits for 1-bit operations. There are no fixed control Qubits, they are different for different operations. The characteristic features of the gate with block diagrams are shown in Fig.6, Fig.7 and Fig.8.

5.1 Two bit logical operations

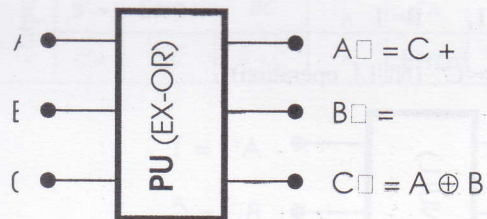
When, **A = 0**, **A' = B AND C** $\frac{(B.C)}{(B + C)}$



A = 1, **A' = B OR C** $(B + C)$
B' = B NAND C (\overline{BC})



C = 0, **C' = A XOR B** $(A \oplus B)$



B = 1, **C' = C XNOR A** $(\overline{C \oplus A})$

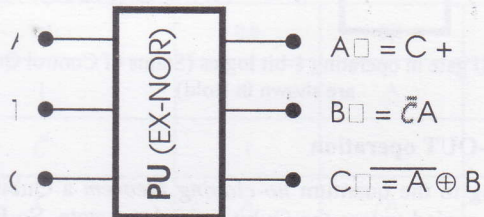
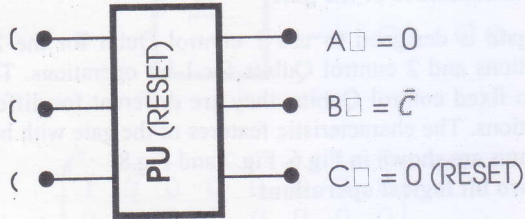


Fig. 6: PU gate in operating 2-bit logics (Status of Control Qubits are shown in Bold)

5.2 One bit logical operations

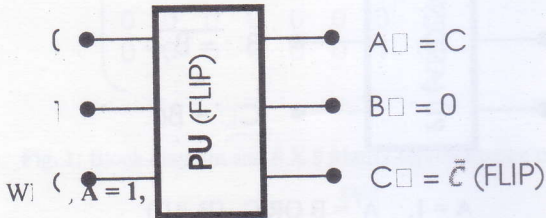
When, **A = 0, B = 0**

C' = 0 (RESET operation)

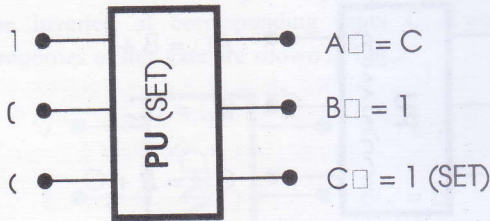


When, **A = 0, B = 1**

C' = C (NOT/FLIP/TOGGLE Operation)



C' = 1 (SET operation)



When, **A = 1, B = 1**

C' = C (NULL operation)

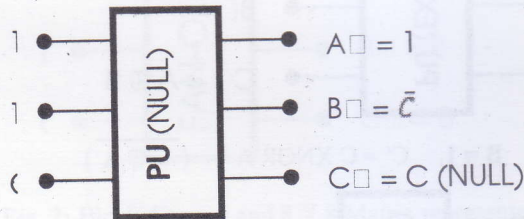


Fig. 7: PU gate in operating 1-bit logics (Status of Control Qubits are shown in Bold)

5.3 FAN-OUT operation

According to the quantum *no-cloning theorem* a Qubit can never be copied unless the Qubit is in sharp state. So FAN-OUT in quantum computer is only possible when it is for the sharp states only. The PU gate in a special sequence of

control bits **B = 0 = C'** allows sharp states to be copied twice at a time, i.e. it works as a level-2 FAN-OUT system.

When, **B = 0, C = 1**

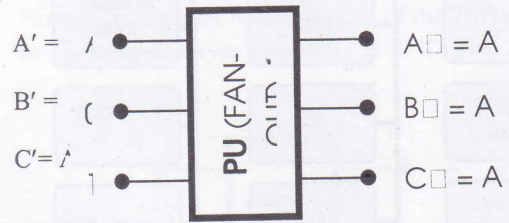


Fig. 8: PU gate in FAN-OUT operational mode (Status of Control Qubits are shown in Bold)

6. Operation and the Truth table of the Gate

The Let, $|\varphi\rangle$ represents an arbitrary 3-qubit input stage as follows

$$|\varphi\rangle = \alpha_{000}|000\rangle + \alpha_{001}|001\rangle + \alpha_{010}|010\rangle + \alpha_{011}|011\rangle + \alpha_{100}|100\rangle + \alpha_{101}|101\rangle + \alpha_{110}|110\rangle + \alpha_{111}|111\rangle$$

Where, $(\alpha_{KKK})^2$ is the probability of $|\varphi\rangle$ being in the stage $|KKK\rangle$

$$\text{So that, } (\alpha_{000})^2 + (\alpha_{001})^2 + (\alpha_{010})^2 + (\alpha_{011})^2 + (\alpha_{100})^2 + (\alpha_{101})^2 + (\alpha_{110})^2 + (\alpha_{111})^2 = 1$$

Generally, during operations, the input/ output states are represented in KET notation (1 column vector notation) like

$$|\varphi\rangle = \begin{bmatrix} \alpha_0 & \alpha_1 & \alpha_2 & \alpha_3 & \alpha_4 & \alpha_5 & \alpha_6 & \alpha_7 \end{bmatrix}^T$$

where, the subscript 0-7 denotes simply the decimal values of the binary states 000-111.

Now, if $|\varphi'\rangle$ be the output, then the operation of the PU gate can be showed by the following matrix operation.

$$|\varphi'\rangle = \begin{pmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{pmatrix} \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \\ \alpha_5 \\ \alpha_6 \\ \alpha_7 \end{bmatrix} = \begin{bmatrix} \alpha_2 \\ \alpha_0 \\ \alpha_1 \\ \alpha_4 \\ \alpha_3 \\ \alpha_7 \\ \alpha_6 \\ \alpha_5 \end{bmatrix}$$

That is, the gate swaps possibilities of being in state 3 & 4, and 5 & 7; keeps the 6th state unchanged; and cycles the probabilities of the states from 0 to 2 to its previous state.

An example operation is shown below for the case of $|\varphi\rangle$ being in the sharp state of $|101\rangle$,

$$\begin{pmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{pmatrix} \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 1 \\ 0 \end{pmatrix}$$

$|101\rangle$ $|111\rangle$

That is, $PU(|101\rangle) = |111\rangle$.

The truth table for all the 8 possible sharp state inputs is shown in Table.1.

Table. 1: Classical Equivalent Truth table for PU gate:

Input Qubits			Output Qubits		
A	B	C	A'	B'	C'
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	1

7. Behavior Analysis and Overall Block Representation

The Boolean behaviors of the PU gate for the sharp state inputs are summarized in Fig.9. The corresponding analysis are shown below.

$$A' = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

Table. 3: Single Qubit logic table

Output Qubits	Control Qubit Status (A, B =)				Control Qubit Status (B, C =)		
	0,0	0,1	1,0	1,1	0,0	0,1	1,0
A' =	0	C	C	1	0	A	A
B' =	\bar{C}	0	1	\bar{C}	1	A	A
C' =	0	\bar{C}	1	C	A	A	\bar{A}

$$\begin{aligned} &= (\bar{A}B + A\bar{B})C + AB(C + \bar{C}) \\ &= C(A \oplus B) + AB \\ B' &= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} \\ &= \bar{B}\bar{C}(\bar{A} + A) + A(\bar{B}C + B\bar{C}) \\ &= \bar{B}\bar{C} + A(B \oplus C) \\ C' &= \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + ABC \\ &= \bar{C}(A\bar{B} + \bar{A}B) + AC(\bar{B} + B) \\ &= \bar{C}(A \oplus B) + AC \end{aligned}$$

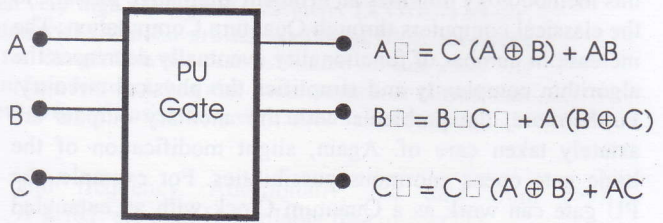


Fig. 9: Overall Block Functional Representation of PU Gate

8. Logic Tables

The In the operations of PU gate, as already seen, none of the three inputs are control input for all the time. It has already shown that, the gate fulfills the design criteria or the fundamental requirements. For further analysis, logic tables for 1-bit and 2-bit are drawn in Table.2 and Table 3 to summarize all the logical processes involved with this gate in different situations.

Table. 2: 2-Qubit logic table

Output Qubits	Control Qubit Status					
	A=0	A=1	B=0	B=1	C=0	C=1
A' =	BC	B+C	CA	C+A	AB	A+B
B' =	Error!	\overline{BC}	$C+A$	$\bar{C}A$	$A+\bar{B}$	$A\bar{B}$
C' =	$B\bar{C}$	$\bar{B}+C$	A	Error!	$A\oplus B$	A

9. Potential of the Gate

The key concern in the designing of the gate was to make it capable of computing all elementary 1-bit and 2-bit classical operations. A Toffoli gate, as pointed earlier, can simulate classical NAND gate and as NAND gate is universal so, obviously any arbitrary classical operations can be achieved with a number of Toffoli gates in a specific arrangement. But, with the proposed gate here, it is possible to have the same Universality with a lot fewer stages (which is a single stage for 1-bit and 2-bit operations). Therefore, this gate or this methodology provides an efficient alternative passage to the classical computers through Quantum Computation. The increase in number of functionality eventually decreases the algorithm complexity and simplifies the physical circuitry. Furthermore, the problems with the ancillary outputs are astutely taken care of. Again, slight modification of the basic gate opens enormous possibilities. For example, the PU gate can work as a Quantum Clock with an entangled feedback circuit. Flip-flops can be prepared with using an additional Pauli-X gate. In this way, it reduces the construction complexity of most of the typical digital circuits like Adder, Multiplier, Divisor, Counter, Register etc.

10. Conclusion

In this paper the proposed PU gate has been vividly presented. Though the system currently functions for some basic operations only, it can be extended for more logic gate operations. At present, no such generic quantum gate exists that can make all the functions with optimum performance. It is not only about the gate, but also about the concept of

preparing such multipurpose gates which is believed to be a great utility in efficient construction.

Therefore, day by day ternary and quaternary logic systems are positioning to be interesting alternatives to traditional binary logic base of quantum computation and hence there is a scope for upgrading the proposed PU gate from binary quantum base to Qutrit and/or Qudit systems. In fact, to realize this gate physically using any hardware standard is obviously the bigger challenge yet to be faced.

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