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Performance Analysis of Metallic Single Walled Carbon Nanotube (SWCNT) in circuit interconnections for VLSI

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Abstract

The Resistor Capacitor (RC) model is used to analyze circuit parameters for a CNT-bundle interconnects. In this paper the performance of the single CNT interconnection with Cu and Au using predetermined equations was attempted first. Due to poor yield of single CNT, bundle of CNT was analyzed and eventually the performance of the CNT-bundle, copper and gold interconnects was compared respectively at local, intermediate and global lengths. Finally it has been shown that the metallic SWCNT gives better performance than copper and gold interconnects for both the intermediate and global dimension.

Keywords: Carbon Nanotube, SWCNT, VLSI, Interconnect.

1. Introduction

Interconnects in an integrated circuit (IC) distribute clock and signal, as well as provide a path for the power supply and the ground. The performance of an IC is determined, to a large extent, by the current carrying capacity and the parasitic resistance and capacitance of these interconnects. The International Technology Roadmap for Semiconductors (ITRS)[1] emphasizes the need for reliable, high-speed interconnects for future technology generations. Common interconnect materials are highly susceptible to electro migration at high current densities ($> 10^6$ A/cm^2) and have lower reliability as the interconnect dimensions are scaled . The resistivity of copper (Cu) and gold (Au) which are extensively used for high performance scaled ICs increases with a decrease in dimensions, due to electron-surface and grain-boundary scatterings[2]. Innovative materials are being extensively studied as replacements for copper and gold and carbon nanotubes (CNTs) have emerged as a promising material for future generation ICs[2].

The resistance of copper and gold interconnects, with cross-sectional dimensions of the order of the mean free path of electrons (~40 nm in Cu and ~50 nm in Au at room temperature) in current and imminent technologies is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of the highly resistive diffusion barrier layer[3]. The steep rise in parasitic resistance of copper and gold interconnects poses serious challenges for interconnect delay especially at the global level where wires traverse long distances and for interconnect reliability , hence it has a significant impact on the performance and reliability of VLSI circuits[4].

In order to alleviate such problems, changes in the material used for on-chip interconnections have been sought even in earlier technology generations, for example the transition from aluminum to copper some years back. Carbon nanotubes have recently been proposed as a possible replacement for metal interconnects in future technologies[5,6] and this paper addresses the performance evaluation of the nanotube bundle in case of local, intermediate and global interconnects.

2. Metallic Single Walled Carbon Nanotube (SWCNT)

Since their discovery in 1991, carbon nanotubes (CNT) have received tremendous research interest as they have many unique mechanical, electrical, thermal and chemical properties[7].

A carbon nanotube is a one atom thick sheet of graphite called grapheme, rolled up into a seamless cylinder with diameter of the order of a nanometer. CNTs exhibit extraordinary strength and unique electrical properties, and are efficient conductors of heat. There are two main types of carbon nanotubes: single walled nanotubes (SWCNTs) and multi walled nanotubes (MWCNTs). In SWCNTs the cylindrical structure consists of a single layer of graphene, while MWCNTs consist of multiple concentric cylinders or the graphene sheet is simply rolled in around itself resembling a scroll of parchment, and are metallic in nature.

SWCNTs are a very important variety of CNT because they exhibit important electric properties that are not shared by MWCNTs. The remarkable properties (Table 1) of SWCNTs stem from the symmetry and unusual electronic structure of graphene . It has a band gap in most directions in k-space, but has a vanishing band gap along specific directions and is called a zero band gap semiconductor. When wrapped to form a nanotube, the momentum of the electrons moving around the circumference of the tube is quantized. The result is either a one dimensional (1-D)

metal or semiconductor depending on how the allowed momentum states compare with the preferred directions for conduction. Metallic SWCNTs have a fermi velocity $v_F = 8\times10^5$ m/s that is comparable to typical metals.

A SWCNT is close to an ideal one-dimensional system of electrons that gives rise to many unique electrical and thermal properties. Since electrons can move in one dimension only, the phase space for scattering in nanotubes is very limited; electrons can be scattered only backward. The mean free path in high-quality nanotubes is in the micron range because when the bias voltage is low there is no high energy phonon scattering. This is in contrast to a three-dimensional metallic wire in which electrons can be backscattered by various small-angle scatterings, and the mean free paths are in the range of a few tens of nanometers. In addition, carbon nanotubes have the potential of being used as both transistors and interconnects since they can be either metallic or semiconducting depending on their chirality[7].

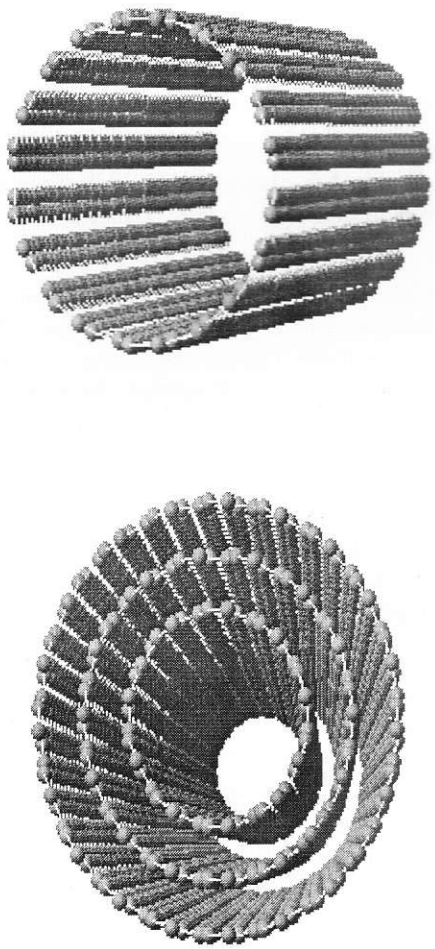


Fig. 1: Single wall and multi wall carbon nanotube[5]

Table 1: Electrical and thermal properties of SWCNTs vs copper and gold

Properties	CNT	Cu	Au
Mean free path (nm) at room temp	>1000 [9]	40	50[10]
Maximum current density (A/cm^2)	$>1x10^{10}$ [9]	$\sim1x10^6$	(0.8-1.15)[10]
Thermal conductivity (W/mK)	5800 [9]	385	318[10]

3. Modeling of SWCNT, Cu and Au Interconnects

A. Resistance of CNT interconnects

There are three contributions towards the resistance of the CNT bundle; Contact resistance, Fundamental resistance, and Ohmic or scattering resistance. Contact resistance is mainly due to imperfect contact between metal and CNT interconnect and it can be as high as 120 K[11] . Fundamental resistance which is given by $h/4e^2$, where h is plank's constant and e is electron charge is present in CNT for all length due to spin degeneracy and sub-lattice degeneracy of electrons in grapheme [12]. Additional, scattering resistance is present for the length greater than the mean free path (>1□m) of CNT[13] as electron movement will no longer be ballistic and it scatters . The total resistance of the CNT bundle is given by:

$$R_{bundle} = (R_C + R_Q + R_S l)/n_{CNT} \quad (1)$$

Where, R_C, R_Q, and R_S are metal contact, fundamental, and ohmic resistances respectively. n_{CNT} is number of metallic CNTs and l is length of interconnect, respectively.

The number of CNTs is calculated using the following geometry:

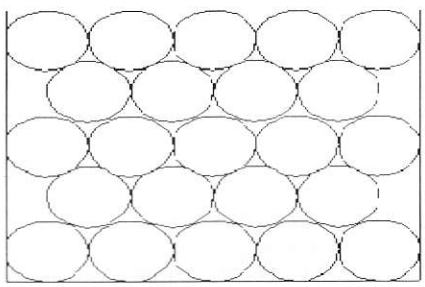


Fig. 2: Hexagonal geometry of a CNT bundle[14]

The hexagonal geometry of CNT bundle is used to comprise maximum number of CNTs in a CNT bundle. Here, the electromagnetic interference among the CNTs is neglected due to the non interacting behavior of CNTs which is assumed.

The number of rows n_W and number of columns n_H are calculated using the following equations[14]

$$n_W = \frac{[w-d]}{x} \quad (2)$$

$$n_H = \left[\frac{h-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right] + 1 \quad (3)$$

where, x is the distance between the centers of two CNTs.

Now, the total number of CNT

$$n_{CNT} = n_w n_H - \frac{n_H - 1}{2}, \quad if\ n_H\ is\ odd \quad (4)$$

$$= n_w n_H - \frac{n_H - 1}{2}, \quad if\ n_H\ is\ odd \quad (5)$$

B. Resistance of Cu and Au interconnects

The resistivity model of any metallic wires with dimensions in the range of mean free path is based on the Fuchs-Sondheimer model for surface scattering of electrons and the theory of Mayadas and Shatzkes for the scattering of electrons at grain boundaries is given by[14]

$$\frac{\rho_s}{\rho_0} = 1 + \left(\frac{3}{4}\right)(1-p)l/w \quad (6)$$

$$\frac{\rho_0}{\rho_g} = 3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 ln\left(1 + \frac{1}{\alpha}\right)\right] \quad (7)$$

$$\alpha = \left(\frac{l}{d}\right)\frac{R}{1-R} \quad (8)$$

$$R = \frac{(\rho_s + \rho_g)l}{wh} \quad (9)$$

Here,

R= resistance of the wire

w= width of the wire

h= height of the wire

ρ_s= resistivity due to surface scattering

ρ_g= resistivity due to grain boundary scattering

ρ_0 = bulk resistivity of metal

p = surface scattering coefficient

R = reflection coefficient at grain boundary

l' = mean free path

d = average distance between grain boundaries

C. Capacitance of CNT interconnects

In CNT, capacitance arises from two sources; quantum capacitance and electrostatic capacitance. The quantum capacitance accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Quantum capacitance is used to model the energy needed to add an electron at an available quantum state above the Fermi level and it is turning out around 400aF/□m[15]. Basic equations for the capacitances of single CNT can be formulated as[14]

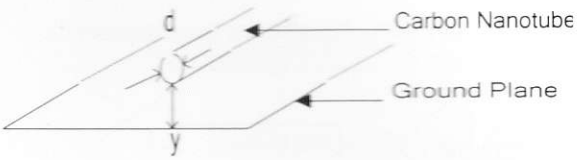


Fig. 3: Isolated conductor, with diameter 'd', over a ground plane at a distance 'y' below it[16]

$$\text{electrostatics capacitance, } C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{2y}{d}\right)} \quad (10)$$

where, ε is the dielectric constant quantum capacitance,

$$C_Q = \frac{2e^2}{hv_F} \quad (11)$$

The total electrostatic capacitance of the bundle can be calculated as electrostatic bundle capacitance,

$$C_E^{bundle} = 2C_{En} + \frac{(n_w-2)C_{Ef}}{2} + \frac{3(n_H-2)C_{En}}{5} \quad (12)$$

Where, C_{En} and C_{Ef} are the intrinsic plate capacitance.

The total quantum capacitance of the bundle can be calculated as $C_Q^{bundle} = C_Q^{CNT}.n_{CNT}$ (13)

Now, the overall capacitance can be calculated as

$$\frac{1}{C_{bundle}} = \frac{1}{C_Q^{bundle}} + \frac{1}{C_E^{bundle}} \quad (14)$$

D. Capacitance of Cu and Au interconnects

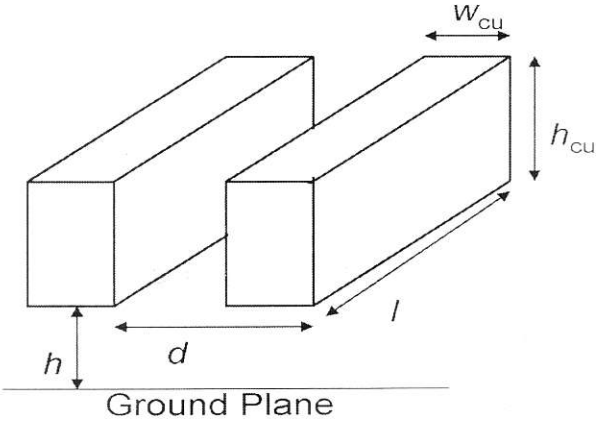


Fig. 4: Layout of parallel Cu interconnects showing the interconnect dimensions.

Note that $h$cu is the height of a Cu wire whereas h is its height from the ground plane[17]

The coupling capacitance between adjacent Cu wires is given by[17]

$$C_c = \frac{\varepsilon h_{cu} l}{d - w_{cu}} \quad (15)$$

The same equation is used for calculating the coupling capacitance between adjacent Au wires.

E. Delay of CNT bundle, Cu and Au interconnects

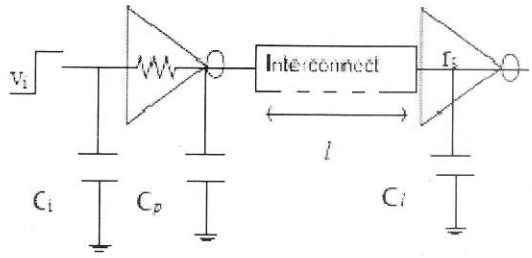


Fig. 5: Schematic of interconnect circuit used for performance evaluation. The "interconnect" is replaced by the equivalent circuit representation for CNT-bundle or Cu interconnect[14]

Delay in VLSI circuit is defined as the difference in the time when the output waveform crosses 50% of its final value and its corresponding time for the input waveform[7]. The delay in VLSI circuit can be calculated in different ways. Here the popular Elmore delay expression[10] is used to obtain the delay of CNT bundle, Cu and Au interconnects. The delay expressions for the equivalent circuit shown in Figure 5. are

$$\tau_{CNT} = 0.69r_s(C_l + C_p) + 0.69\left(r_s + \frac{R_c + R_Q}{2n_{CNT}}\right)C^{bundle} \times l + 0.38\left(\frac{R_s}{n_{CNT}}\right)C^{bundle} \times l^2 + 0.69\left\{\frac{R_s}{n_{CNT}}l + \frac{R_c+R_Q}{n_{CNT}}\right\}C_l \quad (16)$$

$$\tau_{Cu} = 0.69r_s(C_l + C_p) + 0.69r_sC_{Cu}l + 0.38R_{Cu}C_{Cu}l^2 + 0.69R_{Cu}C_l\,l \quad (17)$$

$$\tau_{Au} = 0.69r_s(C_l + C_p) + 0.69r_sC_{Au}l + 0.38R_{Au}C_{Au}l^2 + 0.69R_{Au}C_l\,l \quad (18)$$

Where,

r_s = driver resistance

C_l = load capacitance

C_p = parasitic capacitance

C^{bundle} = bundle capacitance

C_{Cu} = Capacitance of Cu

R_{Cu} = Resistance of Cu

C_{Au} =Capacitance of Au

R_{Au} = Resistance of Au

4. Performance Analysis of CNT, Cu And Au Interconnects

In this section the performance of CNT, Cu and Au interconnects are analyzed in the case of local, intermediate and global dimensions.

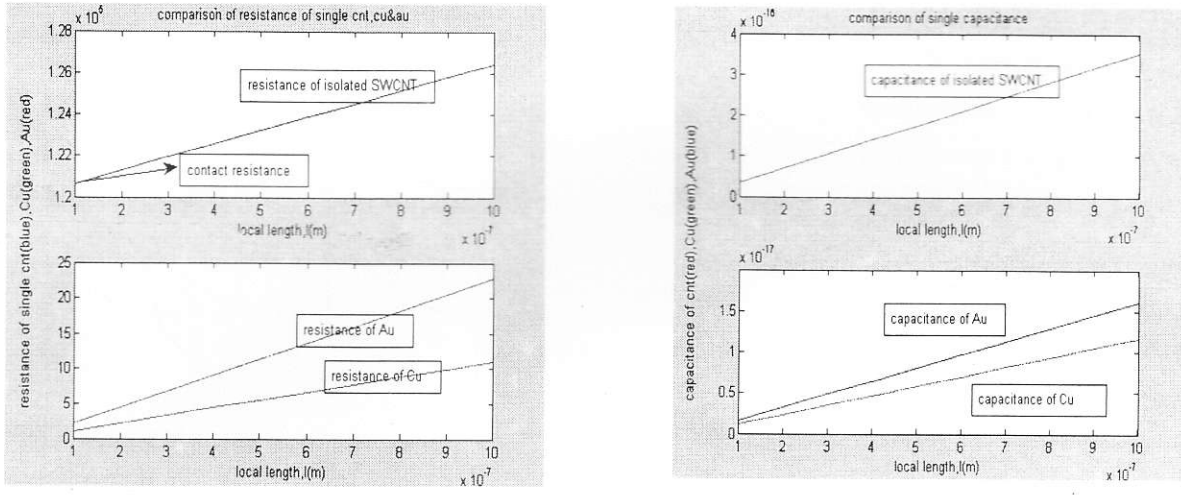
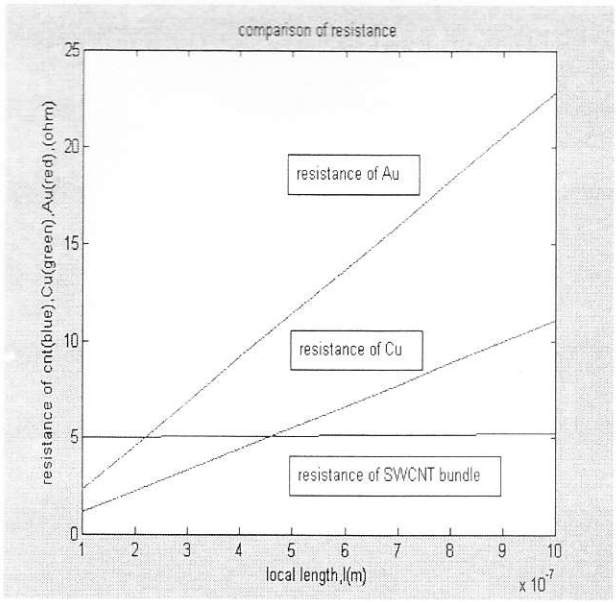
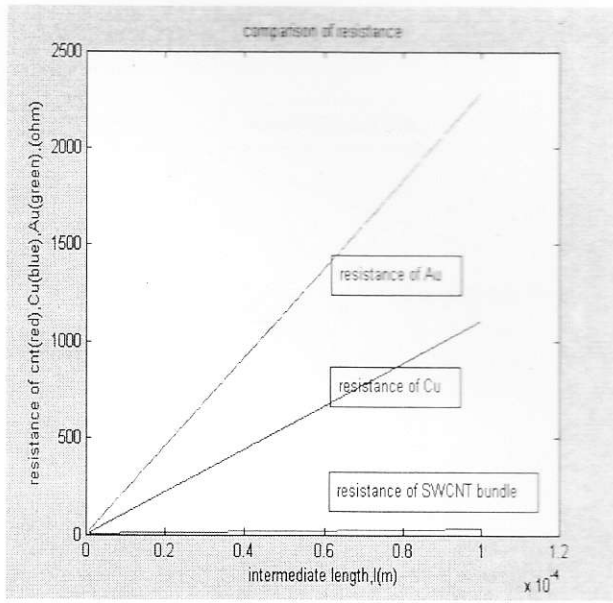


Fig. 6: Comparison of resistance and capacitance among isolated SWCNT, Cu and Au interconnects

From Figure 6. it is seen that in the case of local length, the single SWCNT does not give any satisfactory result neither in resistance nor in capacitance. The resistance is high due to contact resistance which is near about 120 KΩ and quantum resistance which is near about 6 KΩ.The capacitnace effect is high due to electrostatic and quantum capacitance where there is no such effect in case of Cu and Au, that's why they yield better performance.Now for better performance bundle of CNT has been analyzed and compared with Cu and Au interconnects.





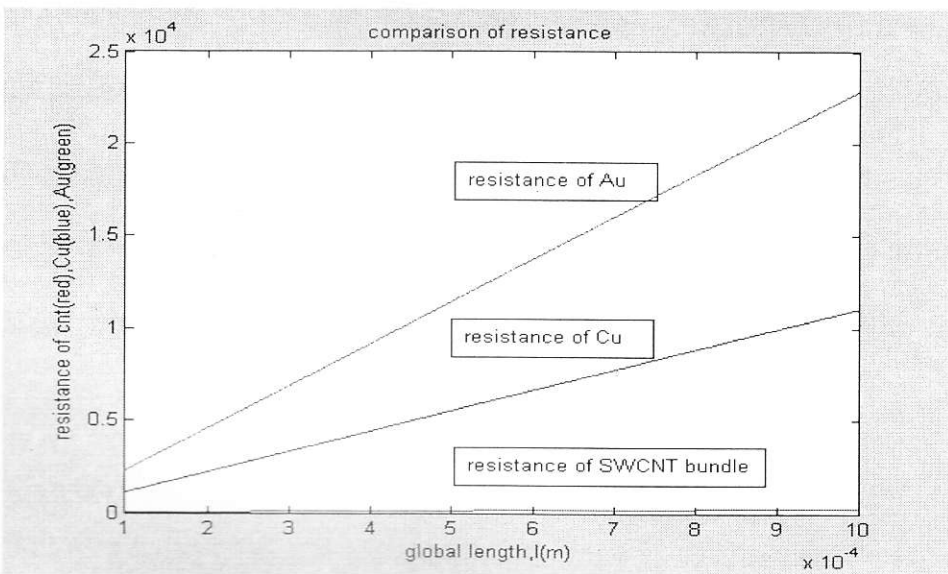


Fig. 7: Comparison of resistance among bundle of SWCNT, Cu and Au interconnects in the case of local, intermediate and global length

From Figure 7. it is seen that in the case of local length, after a certain length the resistance of bundle of SWCNT tends to decrease than Cu and Au interconnects but in the case of intermediate and global length its resistance is much lower than Cu and Au interconnects.The resistance has been decreased because it has been assumed that the SWCNT bundle in parallel geometry in a hexagonal shape.

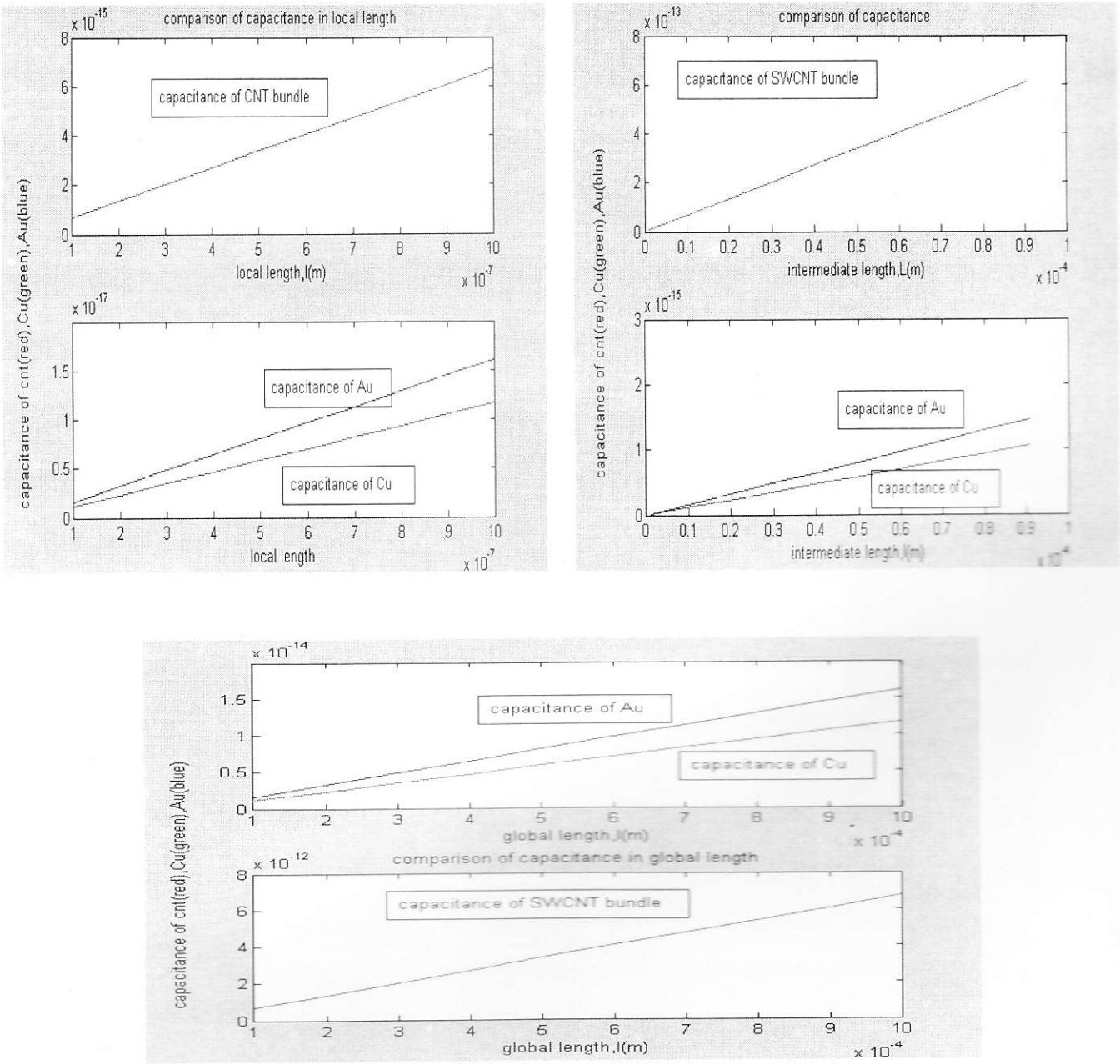
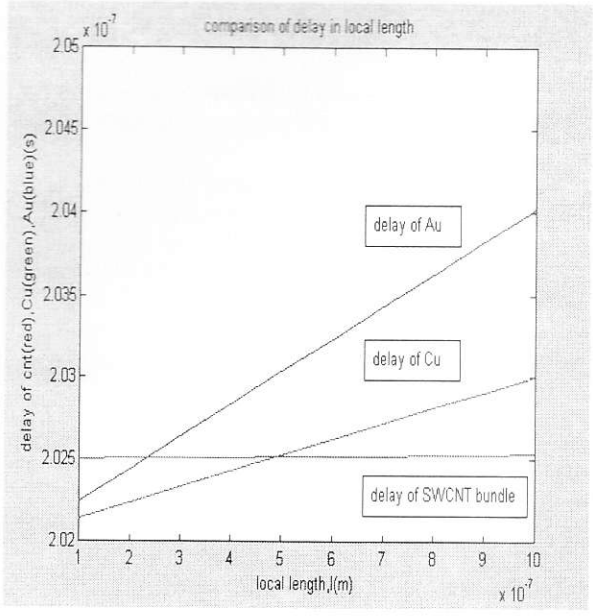
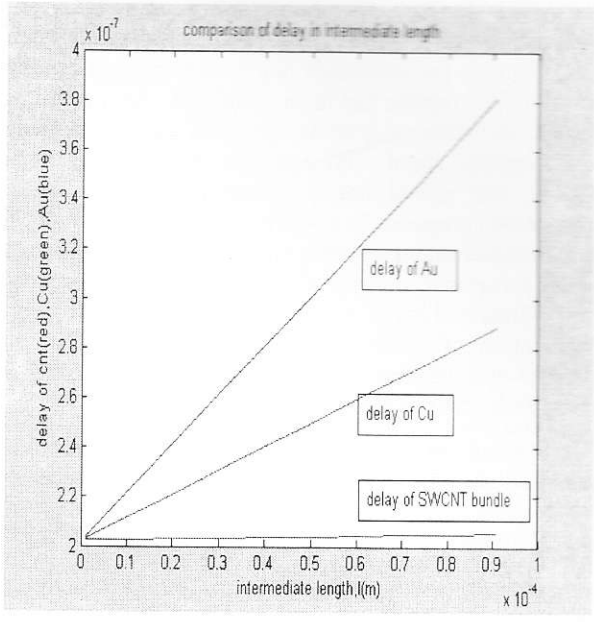


Fig. 8: Comparison of capacitance among bundle of SWCNT, Cu and Au interconnects in the case of local, intermediate and global length

From Figure 8. it can be concluded that the capacitance of bundle of SWCNT is much higher than the capacitance of Cu and Au interconnects in the case of local, intermediate and global length. The capacitance effect of bundle of SWCNT has been increased due to the parallel configuration where capacitance effect of each SWCNT is added significantly.





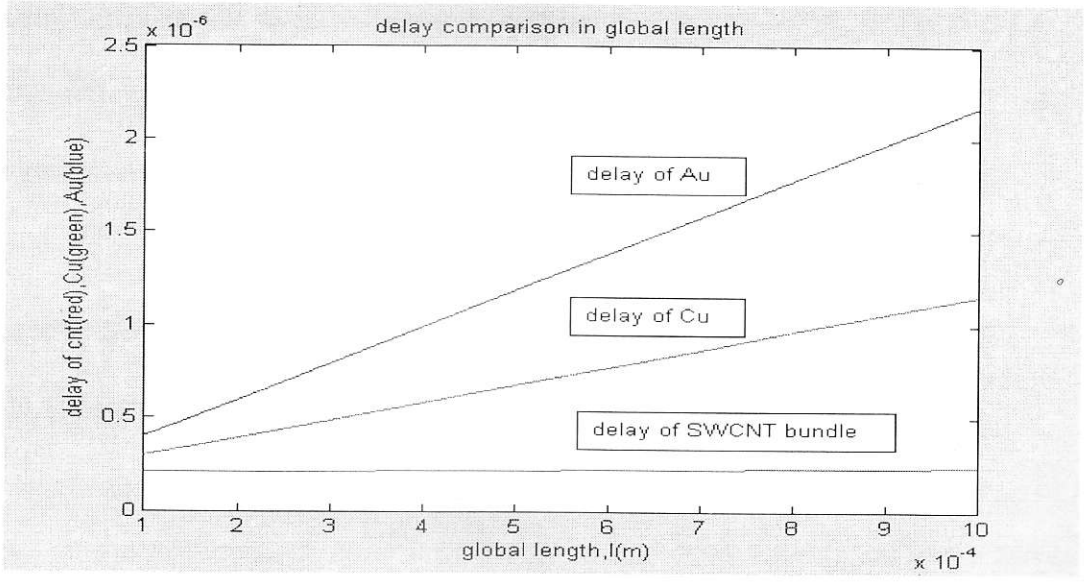


Fig. 9: Comparison of delay among bundle of SWCNT , Cu and Au interconnects in the case of local, intermediate & global length

From Figure 9. it is seen that in the case of local length the delay of bundle of SWCNT tends to decrease after a certain length than Cu and Au interconnects but in the case of intermediate and global length it gives tremendous result than Cu and Au interconnects. Although the capacitance effect of bundle of SWCNT is much higher than the Cu and Au interconnects but the delay is lower than that for RC product.

5. Conclusion

In this paper the applicability of bundle of carbon nanotube has been analyzed as interconnects for future of VLSI technology. The performance of CNT bundle interconnects has been compared with Cu and Au interconnects. At first the performance of single CNT has been shown and compared with Au and Cu interconnects in local length. It has been seen that the single CNT yields poor performance than Cu and Au interconnects. It is due to its contact resistance and quantum reisistace which dominate when the size of the device is so small. For the poor performance in local length, it is not analyzed further interconnecting length.Then the performance of bundle of CNT has been analyzed with Cu and Au interconnects in different

interconnecting length. As the number of CNTs are increased the effective resistance of the bundle has been decreased. Though the resistance has been decreased but the capacitance of the bundle has been increased . As a result in local length, the ultimate goal delay of CNT bundle yields poor performance than Cu and Au interconnects. In intermediate and global length it has been given better performance as compared to copper and gold interconnects in spite of contact and quantum resistance. But here we had to consider an optimal density of CNT bundle where bundle width is 103nm and mean free path is about 1 micron. So any degradation of mean free path length of CNTs and restriction to optimal density of CNT bundle can offset the benefit the using the CNT bundle interconnections.

The future work of this paper will cosider the rigorous charaterization of electromagnetic interactions among the tubes and analyze trade-offs between CNT interconnects power, performance and bandwith density.

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