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Design of a Single Phase Sine-Triangle Pulse Width Modulation Multi-level Inverter using PSIM

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Abstract

Multi-level power converters which provide more than two levels of voltage to achieve smoother and less distorted power conversion, have drawn much attention from the researchers especially in applications involving high voltage and high power utility. In this work, cascaded H-Bridge type single phase seven-level inverter has been designed using vertically shifted carrier signals (VSCS) using sine-triangle pulse width modulation (SPWM) scheme. The designed PWM scheme provides less switching times and better output voltage with reduced total harmonic distortion (THD). Power converter topology and control methods in this paper are examined via computer simulation (PSIM Software) to determine the most suitable design and resulting output waveforms, harmonic spectrums are presented.

Keywords: Multi-level inverter, SPWM, VSCS, THD.

INTRODUCTION

Power-electronic inverters are becoming popular for various applications. Among the power-converters multilevel inverters have attracted much interest from the researchers. The emergence of multilevel inverters has been increased for the last decade. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Multilevel inverters' unique structure allows them to reach high voltages and power levels [1]. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. As the number of levels increases, the synthesized output waveform has more steps, which produces a staircase wave that approaches the desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero [2][3]. As the number of levels increases, the voltage that can be spanned by connecting devices in series also increases. It has been shown that for an n-level inverter, n-1 level-shifted carrier waves are required for comparison with the sinusoidal references [4]. The concept of multilevel inverter involves in utilizing an array of series switching devices to perform the power conversion in a small increase of voltage steps by synthesizing the staircase voltage from several levels of DC voltages [5][6][7]. As the numbers of levels are increased, the amount of switching devices and other components are also increased, making the inverter complex and costly. This is one of the disadvantages of multilevel inverters. A complicated controller with a proper related gate drive circuit is needed to control and synchronize the switching devices. To produce a sinusoidal voltage waveform, a switching scheme must be used that results in a series of voltage pulses that closely approximate a sine wave. One method of switching is called pulse width modulation (PWM). Two widely used PWM schemes for multi-level inverters are carrier-based sine-triangle PWM (SPWM) technique and space vector PWM (SVPWM) technique. In this work, Carrier-based sine-triangle PWM (SPWM) is used which sequences the duration of the on-time from switches to produce an excellent synthesis of a sine wave. This PWM scheme work as follows. The SPWM technique, when applied to multilevel inverters, uses a number of symmetrical level-shifted carrier waves [4]. For an n-level inverter, n-1 carriers with the same frequency, f_c and same peak-to-peak amplitude, A_c are disposed such that the bands they occupy are contiguous. The reference, or modulation waveform has peak-to-peak amplitude, A_m and frequency, f_m and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal; then the active device corresponding to that carrier is switched off. A triggering block for simulation model has been developed for the driving of the inverters' switching circuit made with the Insulated Gate Bipolar Transistor (IGBT).

The advantages of multilevel inverter are the voltage fluctuation (dv/dt) stresses on the switching devices are reduced due to the small increment in voltage steps, reduced electromagnetic compatibility (EMC) when operated at high voltage [5], smaller rating of semiconductor devices [8] and better feature of output voltage in term of less distortion, lower harmonics contents and lower switching losses [9][10]. Among the three topologies of multi-level inverters such as cascaded inverter, imbricated cells multi-level inverter & NPC inverter, Cascaded inverter using vertically shifted carrier signals is chosen due to ease of implementation[11].

DESIGN OF THE SINGLE PHASE 7-LEVEL INVERTER

The 7-level inverter is constructed here using 3 independent full-bridges (H-Bridge) each supplied with a constant dc source. Each of the three sources produces a particular level of voltage and together with the zero level the seven levels of the inverter is obtained.

PWM INVERTER USING VSCS

A very common modulation method known as Pulse Width Modulation (PWM) can be utilized for switching the multilevel inverter. This provides us the following advantages:

- Precise control over the output voltage frequency.
- Control of output power.

- Controlling the RMS value of the voltage output.
- Reduction in the value of Total Harmonic Distortion (THD).

The PWM strategy used here using Vertically shifted carrier signals is based on the very interesting work done by Nikolaus Schibli in his Ph.D thesis [11]. The basic theory of this strategy is described beside:

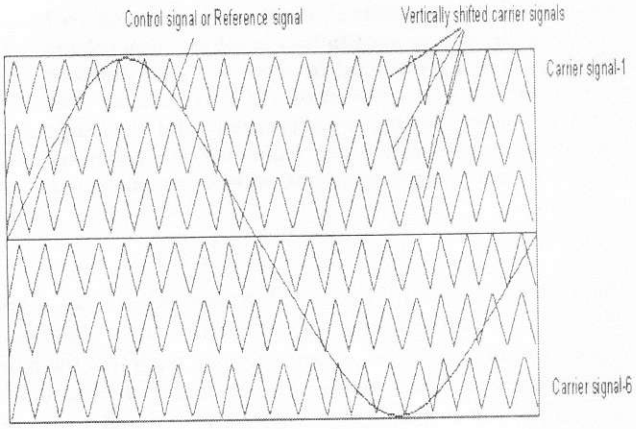

Fig. 1.1: Vertically Shifted Carrier Signals (VSCS)

Instead of having particular switching sequence data the switching times are automatically controlled using a pure sinusoidal waveform as the reference or control signal which is continuously compared with a number of high frequency carrier signals clamped at particular voltages. The number of carrier signals and their amplitude depends on the number of steps desired. The following conditions have to be fulfilled before a successful implementation of the system:

- The offset of each of the carrier signals has to be determined accurately so that no overlapping occurs between the steps; otherwise power loss through unwanted switching will occur.
- All the triangular waveforms have to have the same amplitude and phase.

GENERATION OF THE CARRIER SIGNALS

The following model has been implemented using Power Electronic Simulator PSIM to generate the six carrier signals: Circuit shown in fig.1.2 generates the PWM switching signals using the Reference and Carrier signals for switching the inverter bridges. This system is the subsystem part of the main inverter system from which the three parameters: 1) Modulation index. 2) Phase angle and 3) Carrier frequency (f_c) can be initialized for the system.

The sinusoidal waveform used as Reference signal is generated through the following equation:

Control signal, $Vref = m\_index\ [sin\ (2*pi*50*t + Phase*pi/180)]$ ……(1.1)

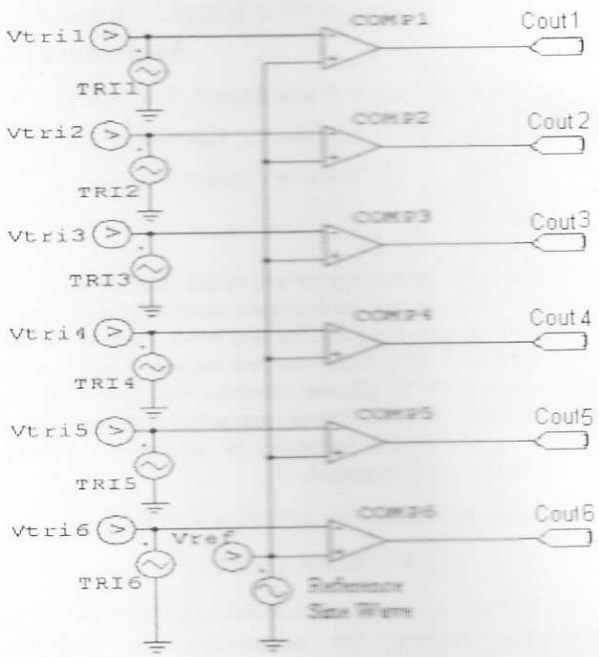

Fig. 1.2: Circuit for generation of the switching signals.

It is clearly understood that the frequency of the control signal is *50Hz* which is the desired frequency of our 7-level inverter. For a single phase inverter the phase angle is considered zero. So above equation can be rewritten as:

Control signal, $Vref=m\_index*sin(2*pi*50*t)$ ..... (1.2)

The control signal is then compared with the carrier signals which are generated using the built-in Triangular signal generators Tri_i where i = 1, 2.... 6. AS in PSIM we have built-in Triangular wave generator, we can use the following information to generate the carrier signals:

Table 1.1: Information to generate the carrier & PWM signals

Parameter	Ref. Signal	Carrier signals					
		1	2	3	4	5	6
Vpp (volt)	1.6	2/6					
Frequency (Hz)	50	800					
Duty Cycle	0.5	0.5					
DC offset (V)	0	4/6	2/6	0	-2/6	-4/6	-6/6
Phase angle (deg)	0	-90					

The output of the above modified carrier signals are given in the following Fig 1.3.

The carrier signals produced are then compared with the generated sinusoidal reference signal using the individual comparators and switching pulses for the legs of each H-Bridges are produced. The six switching pulses to be used for the six legs of the three H -Bridges are also shown in fig 1.4.

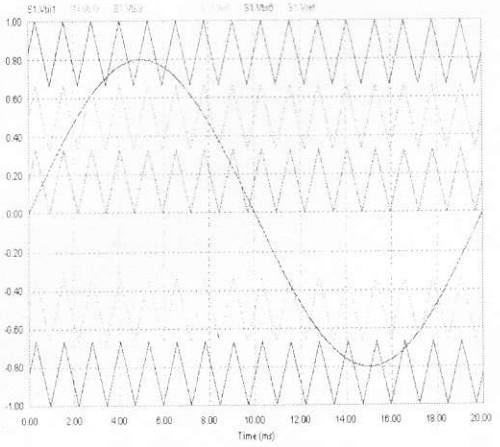

Fig. 1.4: Switching signals for individual legs of each H-Bridge.

The application of the switching pulses from each individual comparator to the legs of the H-Bridge converter is done in such a way so that the pulses generated from the carrier signals that lies in the positive part (signals 1, 2, and 3) as shown in fig 1.3 are fed to those switches of the individual legs of the H-Bridge converter which are responsible for generating a positive voltage. And the signals which are in the negative part (signals 3, 4, and 5) are fed to those switches of the converter that are responsible to generate a negative voltage. Since we have used 3 individual Full bridges each having 4 semiconductor switches. Inverting the outputs of the six switching pulses generates the other pulses. So the signal applied to IGBT1 or IGBT4 is inverted and applied to IGBT2 or IGBT3. These signals are produced using the NOT gates as shown in Fig 1.5. Since both switches of each leg cannot be kept in conducting state simultaneously, this kind of implementation avoids the danger of short-circuiting the H-Bridge converter.

CALCULATION OF DC VOLTAGE SOURCES

Required rms voltage V_{rms}= *230 volts*. So peak voltage that has to be obtained *Vp= 230* × *2 volts = 325.27 volts*. So for each individual H -Bridge required dc source = *Vp/3 = 325.27 / 3 = 108.4 volts (dc)*.

According to the table 1.2 and the inverter circuit shown in the Fig.1.5 to have the bridges switched properly, it can be seen that signal from sequence generator should be connected to the G1, G2 …G6 inputs of the bridge circuits.

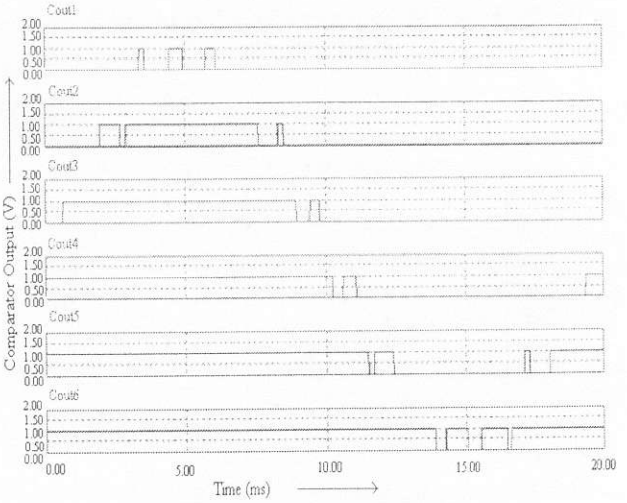

Fig. 1.3: Generated carrier signals.

Table 1.2: Gating signal

V_0(Volts)	G1	G2	G3	G4	G5	G6
0V	0	0	0	1	1	1
108V	0	0	1	1	1	1
216V	0	1	1	1	1	1
324V	1	1	1	1	1	1
324V	1	1	1	1	1	1
216V	0	1	1	1	1	1
108V	0	0	1	1	1	1
0V	0	0	0	1	1	1
-108V	0	0	0	0	1	1
-216V	0	0	0	0	0	1
-324V	0	0	0	0	0	0
-324V	0	0	0	0	0	0
-216V	0	0	0	0	0	1
-108V	0	0	0	0	1	1
0V	0	0	0	1	1	1

The schematic diagram of the single phase inverter using vertically shifted carrier frequency (VSCS) is shown in fig. 1.6.

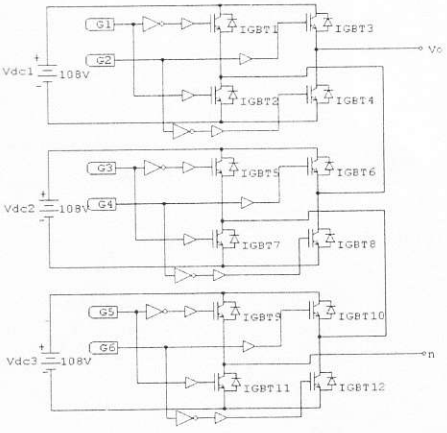

Fig. 1.5: Single Phase PWM multilevel inverter (Showing bridge connection)

In the complete system, the switching signal generator generates the PWM signals to drive the G1, G2... G6 inputs of the Bridges. The output is applied to an inductive load to observe voltage & current response.

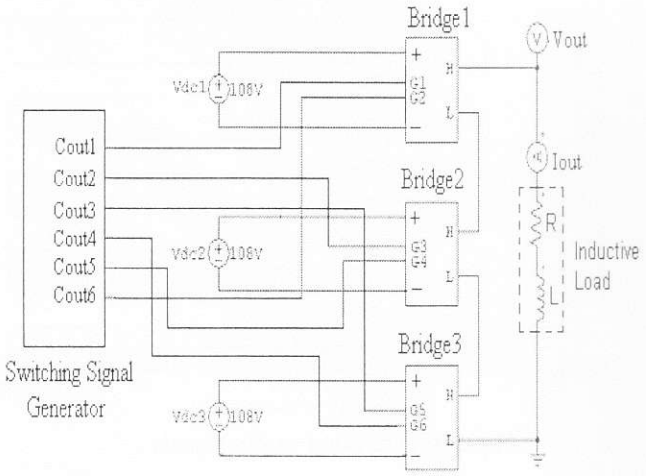

Fig. 1.6: Schematic of the single phase PWM multilevel (ML) Inverter using VSCS.

SIMULATION OF THE INVERTER

Active power: 311W
Reactive power (positive): 305VAR.
Phase load angle: 80.38^0
Carrier frequency used: 800Hz
Frequency modulation ratio: $m_f = 800 / 50 = 16$
Specified modulation index: $A_{Ref}/A_C = 0.8 / 1 = 0.8$
Sample time (Ts) used for simulation: 1×10^{-5} sec.

The output voltage and the current waveform is given in Fig. 1.7

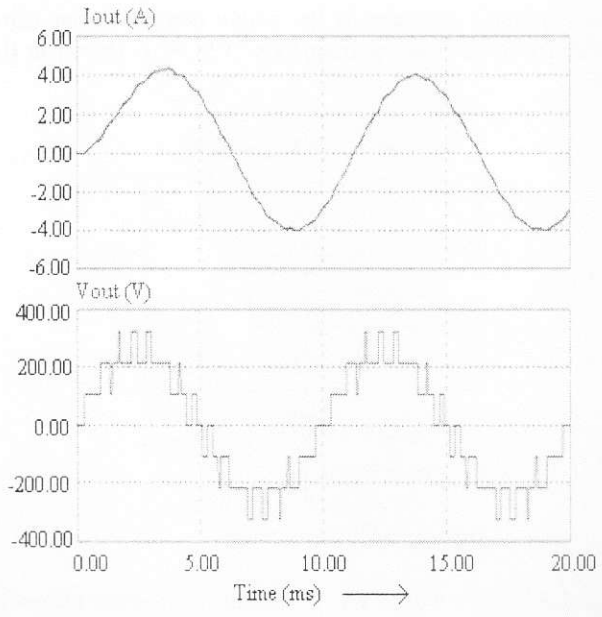

Fig. 1.7: Output voltage and Load current of the 7-Level PWM inverter.

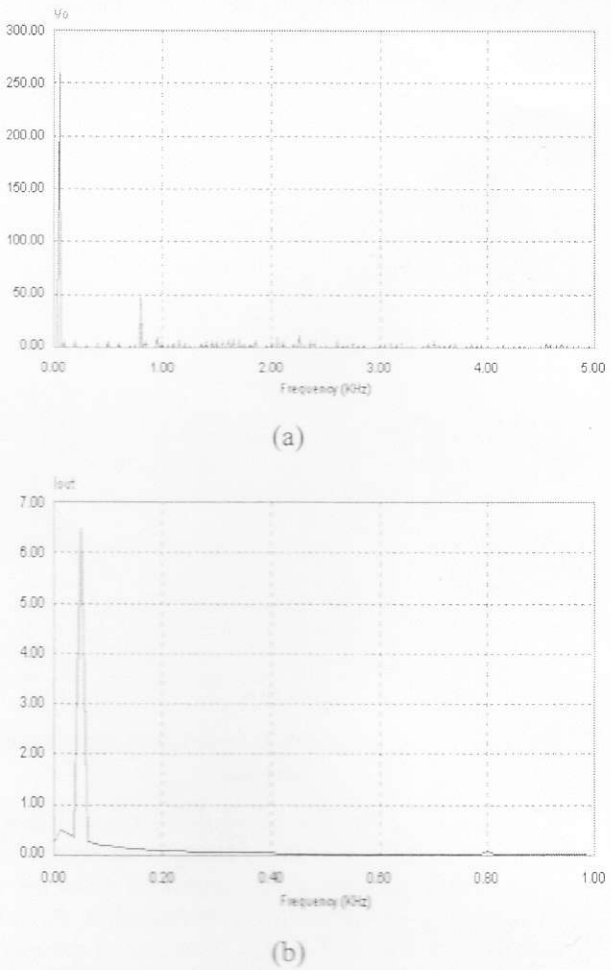

Fig. 1.8: Harmonic contents of (a) voltage waveform and (b) current waveform of ML inverter

The voltage and current outputs are only shown to get an idea of the output response of the PWM inverter. From the voltage waveform characteristic it can be easily observed that by increasing the number of steps of the inverter, the voltage waveform approaches a sinusoidal waveform. At the same time the harmonic content in the waveform decreases.

CONCLUSION

A seven level single phase Sine-Triangle Pulse Width Modulation multilevel cascaded inverter has been designed and a simulation model has been developed for this purpose using PSIM. The performances of multilevel converters are generally assessed based on the spectrum analysis of the generated output voltage and current. The performance of multilevel inverter designed here is satisfactory in terms of output voltage and current spectrum comparing with other inverter topologies. Very low harmonics content in both output waveforms is achieved. It is possible to obtain an acceptable spectral performance with relatively low switching frequency. Increasing the level and number of step size, more reduction in harmonics content is also possible. But increasing levels means number of switching devices required is large, making high cost & complexities for the inverter design. Nevertheless, the recent development in solar inverter, grid-connected inverter and grid-tied inverter increases the necessity of multilevel inverter high because of its low total harmonic distortion.

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