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Online Testable Fault Tolerant Full Adder in Reversible Logic Synthesis

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Abstract

Irreversibility dissipates energy & drives power hungry technology. More liability goes to bit loss recovery. Reversible computing recovers bit loss at input through unique mapping to output and also used in low-power CMOS, quantum computing and optical computing. But bit error is another concern of power consumption and it would be recovered by using fault tolerant technique in reversible computing. In this paper we have proposed fault tolerant full adder with minimum quantum cost and which is also online testable. Online testability provides run time testing facilities to detect bit error. Finally we have shown the experiment result respect to benchmark functions by composing fault tolerant property.

Keywords: bit loss, bit error, fault tolerant, online testable, quantum computing.

1. Introduction

Reversible Computing is only one method to recover bit loss by using unique mapping between input and output. But Irreversible technology dissipates kT*log2 joules of heat energy to reload per bit loss information which has been computed by the author of [1], where k is the Boltzmann's constant and T is the absolute area temperature. Alternatively reversibility disposes of all the undesired intermediate results by retracing the steps of the first stage in backward order and energy dissipation per logical steps is less than kT [2]. In Quantum computing, qubits which preserves the states of each computation [3], the transformation of genetic code from DNA to messenger RNA in Bioinformatics [2] and information encryption are the various fields of use logical reversibility. Reversible computations have some limitations:

1. Fan-out always equal to one
2. Feed back is not permitted

Another fact is the number of garbage's and gates whose have a lower bound to implement the arbitrary output functions [4, 5]. There is a trade between number of gates and garbage outputs. For example, performing same function a circuit may have minimum number of gates but the number of garbage outputs is not optimized or vice versa.

Reversible circuit able to espouse same parity between input-output bit patterns to provide fault tolerance facility. Fault tolerant is divided into two major parts: Error Detection (ED) and Error Correction (EC). Double Error Detection and Single Error Correction are possible if circuit preserves parity [6]. On the other hand Online Testing is the Built-In Self Testing (BIST) method detects bit error at runtime but not able to correct error [15, 16, 17, 18]. In this paper we propose a novel Online Testable Fault Tolerant Full Adder (OTFTFA) by merging both methods which is able to perform fast error detection & correction.

Rest of the paper is organized as follows: Section II discusses about reversible logic, fault tolerant, online testability and quantum realization of reversible logic. Section III presents the relation between parity preserving and online testability. Proposed design of fault tolerant online testable full adder has been described in Section IV. Section V shows the experimental result of fault tolerant realization of Benchmark functions. Section VI finishes this paper with concludes remarks and future study.

2. Background Study

Now a day Reversible Computing is enhanced from various domains like quantum computing, nanotechnology and optical computing etc. Fault tolerant detects error and also provides correction facilities [6, 9]. As well as this paradigm is used to realize most prominent error free Computing Design.

A. Reversible Logic

Reversibility ensures unique mapping between input and output bit patterns where unit logic entity is represented as gates. Reversible gates are used to deploy Reversible circuit which has one to one unique mapping between input and output state.

Let $I_v = (I_1, I_2, \ldots, I_n)$ and $O_v = (O_1, O_2, \ldots, O_n)$ are input and output vectors of a reversible gate, then the relation is $I_v \leftrightarrow O_v$.

There are many popular gates in this literature. For example, Feynman gate (FG) [7], Peres gate (PG) [8], Feynman Double gate (F2G) [9], Toffoli gate (TG) [10] and Fredkin gate (FRG) [11], New Fault Tolerant gate (NFT) [12] are shown in Fig. 1.

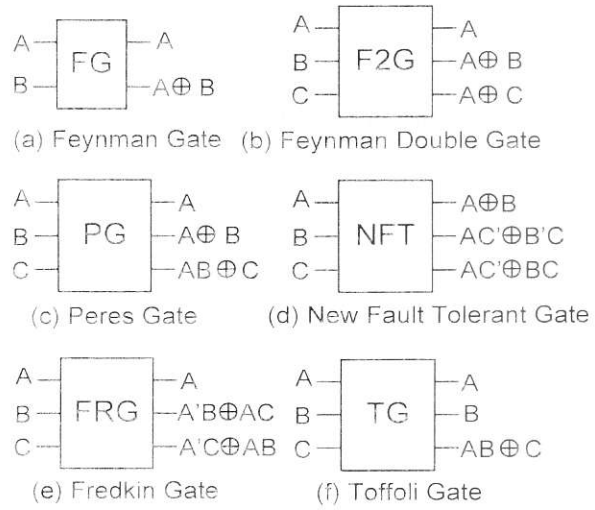

Fig. 1: Reversible Gates with input output mapping function

B. Fault Tolerant Method: Parity Preserving

Parity Preserving (PP) is a property of reversible logic where the input and output vectors of a circuit preserves same parity (odd or even). Consider R is a reversible gate which has unique mapping between input and output vectors should maintain the following constraint to be parity preserving or fault tolerant gate:

$$I_1 \oplus I_2 \oplus \cdots \oplus I_n = O_1 \oplus O_2 \oplus \cdots \oplus O_n$$

In Fig.1 only FRG, F2G and NFT preserve parity and retrain the unique between input-output vectors [12]. Figure 1 shows the reversibility and parity preserving of FRG gate.

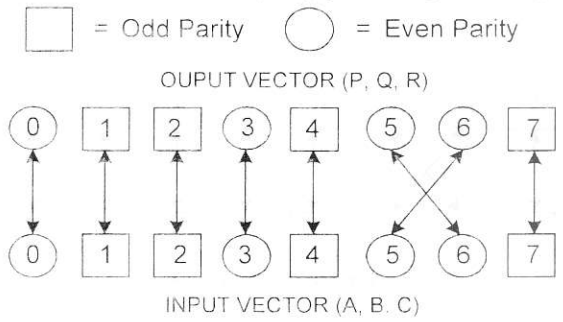

Fig. 2: Input-Output mapping of Fault Tolerant FRG gate

Useful fault tolerant or parity preserving gate is not possible less than 3x3 dimensions [9]. Another IG [13], MIG [14] and Parity Preserving HCG (PPHCG) [6] are newly proposed 4x4 fault tolerant gates as shown in Fig. 3.

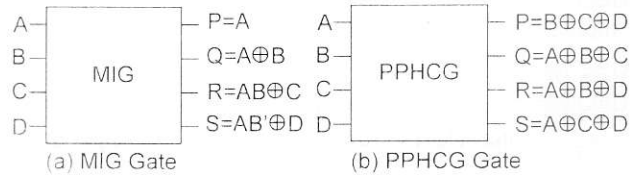

Fig. 3: Two 4x4 dimensional Fault Tolerant Gates

C. Built-In Self Testing: Online Testability

Online Testability uses single output bit to verify alternation of bit at another output lines for a testable gate [15, 17]. An n-dimension reversible gate will be online testable gate if it has following properties [18]:

$$O_n = I_n \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_n \qquad where\ I_n = 0$$

In Fig. 4, R1 and R2 both are Online Testable (OT) gates [16]. To detect error the combination of R1, R2 produces cascading block with two testing Inputs (I_{t1}, I_{t2}) and two testing outputs (O_{t1}, O_{t2}) that satisfy following properties:

$$O_{t1} \oplus O_{t2} = \oplus I_{t1} \oplus I_{t2} \qquad where\ I_{t1} = 0\ and\ I_{t2} = 1$$

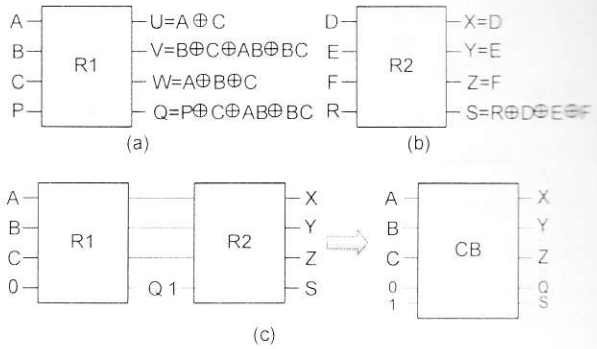

Fig. 4: (a) R1 Testable Gate, (b) R2 Testable Gate, (c) Testable Cascading Block (CB)

In Fig. 4(c), Q and S are the testing outputs whose combination would be impractical respect to desired one if any bit error occurs at other outputs of R1.

Reference [18] used Deduced Reversible Gate (DRG) and Testable Reversible Cell (TRC) to signify Testable Gate and Testable Cascading Block respectively.

D. Quantum Realization: Cost of Circuit

Quantum Realization of reversible circuit is another trend to judge circuit performance and efficiency. Quantum computing uses qubits rather than binary bits and computes multiple operations in a single computation by using matrix operation [3]. Those operations are composed into logical quantum gates which are used to realize reversible circuit. The total number of 2-input quantum gates which are used to realize any circuit is called the Quantum Cost of that circuit. Quantum operations are reversible as reversible circuit operation in Reversible Computing.

Various ways are used to calculate the quantum cost of reversible circuit. The realization process is done by using bidirectional method [4, 5] which is helpful to minimize gate and garbage cost or Computer Aided Design [3]. Reversible XOR operation is equivalent of Controlled-NOT operation of quantum circuit and NOT operation is the multiplication of two pauli – x gate [3] or Quantum NOT (i.e. V). For that, V is called Square Root of NOT (SRN) gate and V^+ is Hermitian of V that produces VV^+=Identity Matrix.

Equivalent quantum circuit of popular reversible gates is shown in Fig. 5.

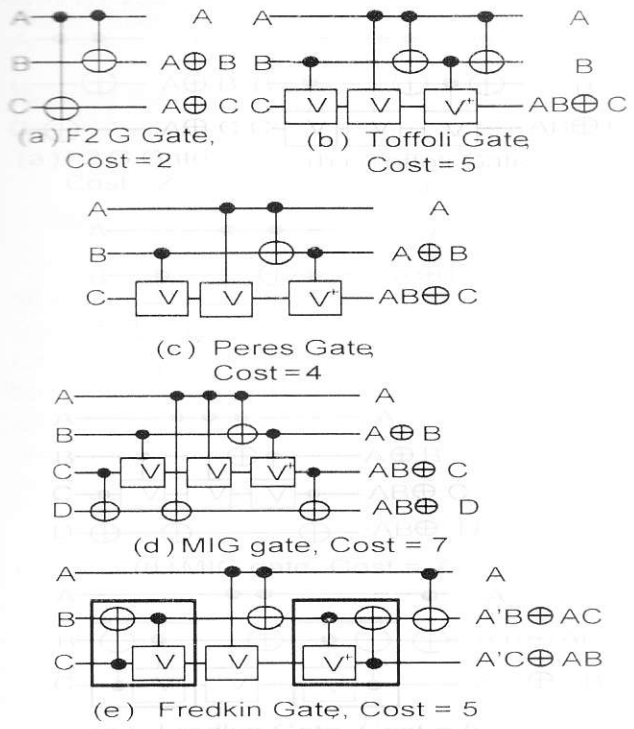

Fig. 5: Quantum realization of Reversible gates

3. Fault Tolerant Online Testable Circuit Design

Online Testing is Built-In Self Testing which only detects error but correction can be covered by using Fault Tolerant circuit. Any n-dimension reversible gate can be Deduced Reversible Gate (DRG) by adding extra input bit(s) and corresponding output bit(s) [18]. But DRG loses the fault tolerant property due to provide online testability.

Theorem 1: Any DRG can never be a Parity Preserving Gate.

Proof: Let, R is a Parity Preserving reversible gate which input and output vectors $I_v = (I_1, I_2, ..., I_n)$ and $O_v = (O_1, O_2, ...O_n)$ where $I_v \leftrightarrow O_v$ that maintains the following rule:

$$I_1 \oplus I_2 \oplus \cdots \oplus I_n = O_1 \oplus O_2 \oplus \cdots \oplus O_n \quad (1)$$

On the other hand migrated DRG can be generated by adding extra bit and mapping would be $I_v(I_1, I_2, ..., I_{n+1}) \leftrightarrow O_v (O_1, O_2, ...O_{n+1})$ where

$$I_1 \oplus I_2 \oplus \cdots \oplus I_{n+1} = O_1 \oplus O_2 \oplus \cdots \oplus O_{n+1} \quad (2)$$

$$O_{n+1} = I_{n+1} \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_{n+1} \quad (3)$$

So according to (2) and (3), we will get

$$I_1 \oplus I_2 \oplus \cdots \oplus I_{n+1} = I_{n+1} \quad (4)$$

But (4) is not true. Hence any DRG can never be a Parity Preserving Gate.

But it is possible to build Fault Tolerant Online Testable Reversible Block (CB) [15, 16 and 17] which can be produced only from fault tolerant gates.

Theorem 2: Any NxN Parity Preserving Reversible gate can be migrated into a (N+2)x(N+2) Fault Tolerant Online Testable Block or Testable Reversible Cell.

Proof: Let R be an NxN Parity Preserving Reversible gate with input-output vectors mapping: $I_v (I_1, I_2, ..., I_n) \leftrightarrow O_v (O_1, O_2, ...O_n)$, so the migrated Testable Reversible Cell will justify $I_v (I_1, I_2, ..., I_{n+2}) \leftrightarrow O_v (O_1, O_2, ...O_{n+2})$ where

$$O_{n+1} = I_{n+1} \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_n \quad (5)$$

$$O_{n+2} = I_{n+2} \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_n \quad (6)$$

By Applying XOR operation between (5) and (6), we get the following relation.

$$O_{n+1} \oplus O_{n+2} = I_{n+1} \oplus I_{n+2} \quad (7)$$

Equation (7) shows that the testing input and output bits of TRC preserve parity. So (N+2) x (Nx2) TRC would be fault tolerant if and only if it is generated by NxN parity preserving Gates.

Finally, Deduced Reversible Gates (DRG) is not Fault Tolerant but corresponding Testable Reversible Cells (TRC) [18] preserve parity according to Theorem 1 and 2.

For example, the FRG Generator (FRGG) and the FRG Propagator (FRGP) are equivalent to DRG whose are not fault tolerant but Online Testable (shown in Fig. 6(a) and 6(b)). The combination of FRGG and FRGP constructs Fault Tolerant Testable Reversible Cell of FRG (FRG TRC) which is shown in Fig. 6(c) which is fault tolerant.

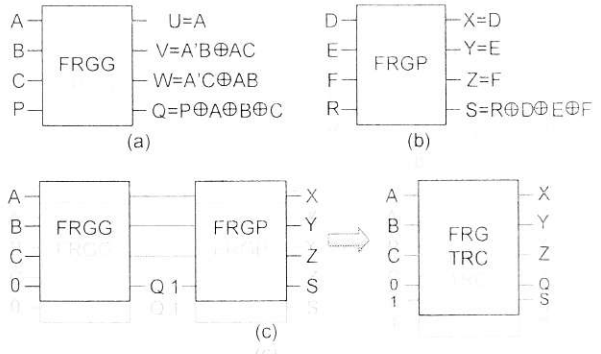

Fig. 6: Quantum realization of Reversible gates

4. Proposed Onlinetestable Fault Tolerant Full Adder

Full Adder is the most imperative circuit for computation which has three inputs (a, b, c_{in}) and output functions are Sum (sum) and Carry (c_{out}) with the following mapping:

$$sum = a \oplus b \oplus c_{in}$$

$$c_{out} = ab \oplus bc_{in} \oplus ac_{in}$$

Next algorithm is proposed to build a Fault Tolerant Full Adder (shown in Fig. 7) with lowest quantum cost by using

minimum dimension of fault tolerant gates which is easily adoptable into minimum dimension of Online Testable Block.

Algorithm 1: Construction of Fault Tolerant Full Adder.

Input : a, b, c_{in}.

Output : sum, c_{out}

begin

1. Generate ($a \oplus b$) by F2G gate
2. Make two copies of c_{in} by another F2G gate
3. Propagate ($a \oplus b$) and generate c_{out} by FRG using c_{in}
4. Generate Sum by XORing ($a \oplus b$) with c_{in} by final F2G.

End

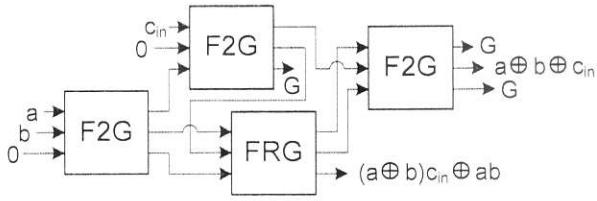

Fig. 7: Proposed Fault Tolerant Full Adder

Table I, shows the comparative performance with existing proposed circuit according to quantum cost. It is better to realize circuit using minimum dimensional reversible gate. Greater dimension causes greater quantum cost.

Table 1: Comparison with existing circuit

Fault Tolerant Full Adder Design	Total Gates		Total Garbage	Quantum Cost
	3x3	4x4		
Proposed	4	0	3	11
Existing[14]	0	2	3	14
Existing[19]	6	0	6	18
Existing[20]	4	0	3	20

The Online Testable version of the above circuit including Fault Tolerant feature is shown in Fig. 8.

Algorithm 2: Design of Online Testable Fault Tolerant Full Adder.

Input : a, b and c_{in}

Output : sum = ($a \oplus b \oplus c_{in}$) and

c_{out} = ($ab \oplus bc \oplus ca$)

Begin

1. Adopt all required 3x3 reversible F2G and FRG gates into 5x5 TRC.
2. Set testing input $I_{t1} = 0$ and $I_{t2} = 1$ of all Testable Blocks.
3. Set connection according to Algorithm (1) which generates c_{out} from FRG TRC and sum from final F2G TRC.

End

5. Experimental Result

We have realized the calculation of proposed algorithms for migrating any circuit into fault tolerant property by using programming language Java (J2SE 1.6.0 17) on Netbeans IDE (6.8) in Linux Workstation. All the experimental results are tested on Intel(R) Core(TM)2 Duo CPU E7300 2.66GHz edition with 2 GB RAM. During the execution, it was ensured that no other application is running. Table II shows the experimental results for different benchmark functions.

Table 2: Experimental Result of Fault Tolerant Realization of Benchmark Functions

Benchmark functions		Proposed Design		
	In/out	GT	GB	QC
5xp1	7/10	166	194	500
9sym	9/1	427	486	1506
adr1	2/2	5	7	12
adr2	4/3	24	32	60
adr3	6/4	67	85	195
apex1	45/45	3929	4216	12670
apex3	54/50	3998	4245	11102
b12	15/9	159	193	514
bw	5/28	305	322	704
clip	9/5	492	569	1813
con1	7/2	35	49	108
cordic	23/2	12162	12958	44008
duke2	22/29	941	1009	3078
Inc1	½	1	0	1
Inc2	2/3	4	5	10
Inc3	8/7	9	11	24
Inc4	4/5	16	10	34
Inc5	5/6	23	33	70
Misex1	8/7	88	104	246
Misex2	25/18	199	234	92
Misex3c	14/14	6259	9793	24641

6. Conclusion

Reversible logic is an emerging research area. This paper has present the idea of using fault tolerant mechanism with online testability and also has proposed minimum cost fault tolerant full adder circuit. The comparison table (Table I) has shown the better performance than previous all design of fault tolerant full adder circuit. An experimental overview on benchmark circuit has been presented finally. We also continue to work on improvement of this research such as quantum computing and other digital circuits.

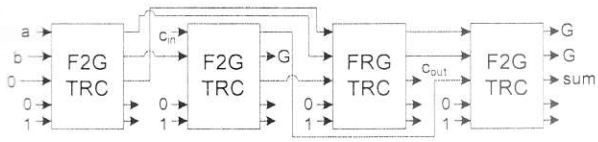

Fig. 8: Proposed Design of Fault Tolerant Online Testable Full Adder

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