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Formation of N-Type Layer upon Silicon Wafer Using $POCl_3$ Diffusion Process

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ABSTRACT

The application of N-type layers, formed upon P-type layers, has a huge impact on the solar cell industry. The formation process of N-type layers (Emitter) upon both side of monocrystalline P-type silicon wafers (Base) using $POCl_3$ (Phosphorus Oxychloride) diffusion process has been investigated and discussed in this paper. Both side as-cut P-type silicon wafers have been used as the substrates. The diffusion procedure has been carried out at 875°C in a $POCl_3$ diffusion furnace using $POCl_3$, N_2 and O_2 gas. The main goal of this research is to find out a low-cost N-type layer fabrication method with a standard sheet resistance value of 40 Ω/sq - 90 Ω/sq. By experimental trials, attempt has been made to reduce the cost by minimizing the utilization of $POCl_3$. The utilization of $POCl_3$ gas has been minimized by decreasing the deposition time and compensating it with using increased drive time by means of low cost N_2 gas. By varying the deposition time, a number of experiments have been done to get the optimum deposition time and drive time. During the diffusion process, the deposition time and drive time variations were 5, 10, 20, 30 min and 10, 15, 25 and 35 min, respectively. Thermal oxidation has been applied after diffusion process. The formation of N-type layer has been confirmed by hot point probe experiment. Furthermore, sheet resistance has been determined experimentally using four-point probe measurement equipment. In addition, electron concentration of the substrate has been calculated. With 5 KeV and 20 KeV accelerating voltage, elements of the fabricated layer have also been analyzed with Energy Dispersive X-ray Spectroscopy (EDS). Remarkably, 65.25 Ω/sq sheet resistance has been obtained with 5 min diffusion and 10 min drive time. Utilization of 5 min diffusion and 10 min drive time recipe can be a low cost procedure for the creation of N-type layer and it is proposed to be used for the solar cell industry.

Keywords: Sheet Resistance; Deposition time; Drive time; Monocrystalline P-type silicon wafer

1. Introduction

Since the discovery of the P-N junction by Russell Ohl in 1940 science has come a long way [1]. In general, a P-N junction can be fabricated by creating an N-type layer upon a P-type layer with donor implantation or thermal diffusion technique [2]. This N-type layer formation plays an influential role in the solar cell industry. So far, 95% N-type layer of solar cells is fabricated on P-type silicon because still, more than 90% of the solar cells produced today are crystalline silicon [3]. Furthermore, according to Industry Technology Roadmap for Photovoltaics (ITRPV) prediction, this dominance will continue by 2026 with over 65% of industrial silicon solar cells fabricated using P-type substrates. Depending upon the surface condition of the monocrystalline silicon, the wafer is categorized as polished and as-cut wafer. Both polished and as-cut monocrystalline wafers are commercially available in the market. In this work, due to avialiabilty and low cost both side as-cut monocrystalline P-type silicon wafer has been selected as the substrate.

Since the 1970's phosphorous diffusion has been the unofficial standard for N-type layer formation. Initially solid P_2O_5 has been used as a dopant source [4]. Later, due to better control, low cost, uniformity, good stability and high throughput of the available production equipment, diffusion using liquid $POCl_3$ (Phosphorus Oxychloride) has been utilized more as dopant source instead of solid P_2O_5. Currently, tube furnace diffusion using $POCl_3$ is the dominating technology for N-type layer formation in P-type silicon solar cells [5]. Thus, in this research $POCl_3$ diffusion furnace has been used for the formation of N-type layers (Emitter) upon both side monocrystalline P-type silicon wafers (Base). This phosphorous diffusion research using $POCl_3$ diffusion furnace has been carried out in one and only monocrystalline silicon solar cell laboratory, Atomic Energy Research Establishment (AERE), Savar, Bangladesh.

The $POCl_3$ diffusion process has been studied extensively by various research groups and the research is still going on [6-12]. $POCl_3$ thermal diffusion process is conducted by either one-step or two-step process [13]. In the one-step process, phosphorous dopant atoms are introduced at the wafer surface in a single stage called $POCl_3$ deposition. Although the one-step process is fast, it deteriorates the electrical performance by creating a heavily doped N-type layer [14-15]. Whereas, in the two-step process after $POCl_3$ deposition, an additional stage called drive-in is used to drive the phosphorous dopants from phosphosilicate glass (PSG) to deeper into the silicon substrate. For overall performance and timing, this paper focuses on the two-stage $POCl_3$ thermal diffusion process. Shen *et al.* used 1100 sec (18.3 min) for deposition and 15 min drive time. Furthermore, Shen *et al.* changed the drive-in time several times but in all the cases drive-in time was less than deposition time [16]. Whereas, XinRui AN in his Doctoral Thesis, mentioned using 15 min for deposition and 10 min for drive time [17]. In addition, Li *et al.* 25 min for deposition and 40 and 80 min for drive time [4]. From these observations it is perceived that, there is no standard deposition and drive time yet. The main goal of this

research is to reduce the cost of fabrication but forming an N-type layer with standard sheet resistance of 40 Ω/sq - 90 Ω/sq [16, 18-19]. Reduction of cost can be done by reducing the utilization of the $POCl_3$ gas by optimizing the deposition time and compensating it using increased drive time with low cost N_2 gas. Therefore, in all the experiments discussed here, the drive time was 5 min more than deposition time. During the experimentation of the diffusion process, the deposition time and drive time variations were 5, 10, 20, 30 min and 10, 15, 25 and 35 min, respectively. After the drive-in stage, an additional stage (shown in Figure 1) called thermal oxidation has been included for surface passivation. After the diffusion process, the hot-point probe experiment was executed to check whether N-type layer has been formed or not.

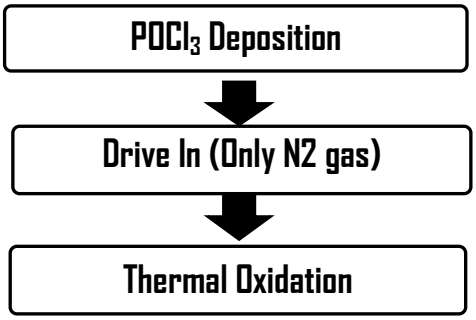

Fig. 1. Stages of Diffusion Process

Due to high phosphorous concentration electrically inactive phosphorous atoms form a dead layer on the P-type layer; that hinder the electrical performance of the solar cell [20].The formation of dead layer in the emitter (N-type) is decided by the sheet resistance value. Therefore, the sheet resistance value of the N-type layer has been determined using Kithlink four-point probe measurement equipment. Furthermore, from the sheet resistance values, electron concentration has been theoretically calculated. Elemental analysis has also been done by using Energy Dispersive X-Ray Spectroscopy (EDS), and all the results are presented and discussed in this paper.

2. Experimental

2.1 Preparation and Wafer Selection:

For the fabrication of the N-type layers, boron (B) doped both side as-cut monocrystalline silicon P-type wafers (Rena Sola, China) were used in this research. Due to the availability and because of the best efficiency of the solar cell, the monocrystalline silicon wafers were chosen for the fabrication process. According to the specification, the pseudo-square as-cut monocrystalline silicon wafer's, crystal orianation, thickness, area, and sheet resistance were (1 0 0), 180±20 μm, 150×150 mm^2, 1-3 Ω.cm respectively [21]. The as-cut wafers are called 'as-cut' because the silicon wafers surface were damaged due to the action of the saw. So, to remove the saw damage and to clean the wafers, the wafers were submerged in 10% NaOH solution at 70-80°C for 10 min. Then the wafers were dried with air-guns. To reduce reflection, the texturization process was carried out in KOH-IPA solution with 0.76 wt% KOH-4 wt% IPA concentration. The texturization process time and temperature were 20 min and 70-80°C respectively [22-23]. Once the texturization process was done the wafers were dried again with air-guns. Then the textured wafers were inserted in the $POCl_3$ diffusion furnace to grow the N-type layers upon the P-type substrates.

2.2 Operation of $POCl_3$ diffusion furnace

At first, the $POCl_3$ furnace system was turned on. When the chamber temperature had reached 200°C, N_2 purge was turned on. Here, nitrogen purge was used to provide contamination and moisture-free inert environment inside the diffusion chamber. Then when the temperature had reached 700°C, the P-type wafers were loaded into the chamber as shown in Figure 2.

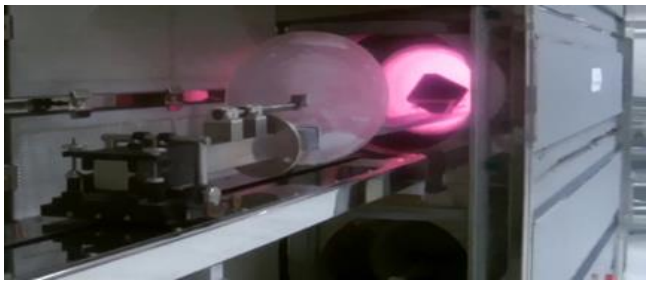

Fig. 2. Insertion of Wafer into the Furnace

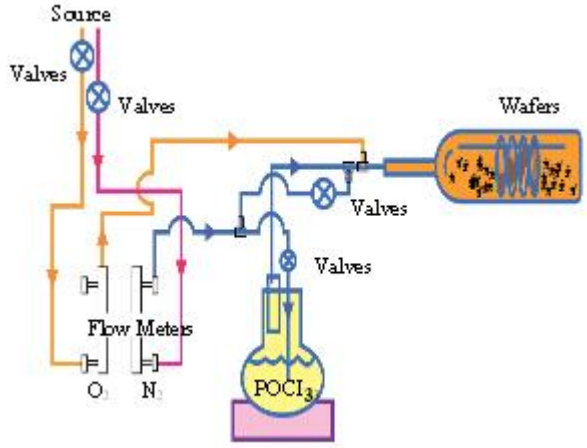

Fig. 3. $POCl_3$ Diffusion Furnace

In general, the deposition process is carried out at 800-900°C [24]. Interestingly, several researchers have found 875°C is good for the diffusion process [25-28]. Thus, 875°C was chosen for the deposition process. On reaching the chamber temperature at 875°C, the deposition process was started by turning off N_2 purge and turning on N_2 source and O_2 source for 5 min each in a subsequent manner. It should be mentioned that the N_2 source was connected to a 2000cc bubbler filled with liquid $POCl_3$ (as shown in Figure 3). Thus, by turning on the N_2 source, the carrier N_2 gas was flown through the bubbler and gaseous $POCl_3$ was produced. Hence, $POCl_3$ vapor went to the chamber which was needed for phosphorous deposition. During the deposition stage, the carrier O_2 gas (provided by O_2 source) was also flown into the $POCl_3$ diffusion furnace. Oxygen gas reacted with $POCl_3$ vapor to create P_2O_5 film in the deposition stage, which were

necessary to form the phosphorous layers upon the P-type wafers.

Moreover, N_2 and O_2 gas flow rate were adjusted to 14.7 psi (Pounds per square inch) to have an atmospheric environment. After 5 min, N_2 and O_2 sources were turned off by setting the flow meter to zero, and N_2 purge was turned on again (which only provides N_2 gas) for 10 min for the drive-in process. In this N_2 purge duration, the N_2 gas (carrier gas) served as a medium for transporting phosphorus molecules tobe deposited on P-type layers and drove the phosphorous dopants from phosphosilicate glass (PSG) deeper into the silicon substrates.

After the completion of the drive-in process, thermal oxidation stage was started. In this stage, N_2 purge was turned off and the O_2 source was turned on for 10 min, which caused the formation of SiO_2 layer over the surface resulting surface passivation by reducing the dangling bonds. Then, O_2 source was turned off and N_2 purge was turned on again for 10 min, to purge the reactive gases from the $POCl_3$ diffusion furnace and also to have contamination and moisture-free diffusion chamber [29]. During the last N_2 purging, the temperature was lowered to 700°C and the wafers were pulled out from the chamber (Figure 4). Lastly, the temperature was lowered to 200°C and the system was turned off. The wafers were cooled down for 30 min. During the operation, the flow rate of N_2 and O_2 were 200 sccm. The process steps and timeline is shown in Figure 5. The whole process was done several times with varying deposition and drive time. The experimentally conducted deposition and drive-time were 5 min-10 min, 10 min-15 min, 20 min-25 min, and 25 min-30 min, respectively.

Fig. 4: Phosphorus Doped Wafer Unloaded From Furnace

2.3 Characterization

In the world of materials science, the word characterization involves knowing any physical, electrical, mechanical or chemical properties of a material. Characterization of a material is done for understanding the behavior of a material and it also helps to explain and improve the parameters of a material. In this work, three types of characterization process such as N-type and P-type semiconductor determination, sheet resistance measurement and elemental analysis by EDS were performed.

2.3.1 N-type and P-type Semiconductor Determination

Recognition of N-type & P-type semiconductor was performed by the "hot point probe" experiment. To do the hot point probe experiment a multimeter's positive and negative leads were placed upon the substrate (N-type or P-type semiconductor) [30]. Then a soldering iron tip was placed very close to the positive lead of the multimeter (as shown in Figure 6). Next, the soldering iron and the multimeter were turned on, the multimeter showed voltage/current reading. After that the multimeter leads and the soldering iron tip were moved to several points and readings were taken accordingly.

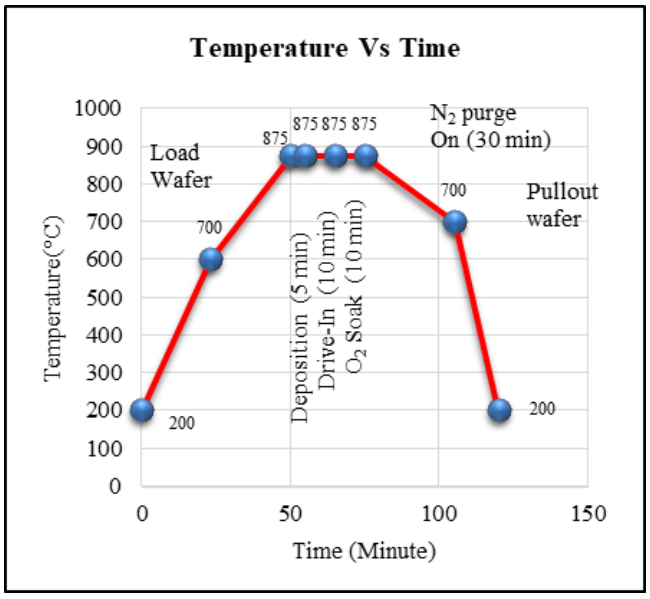

Fig.5: Temperature and Timing Graph of Diffusion Process

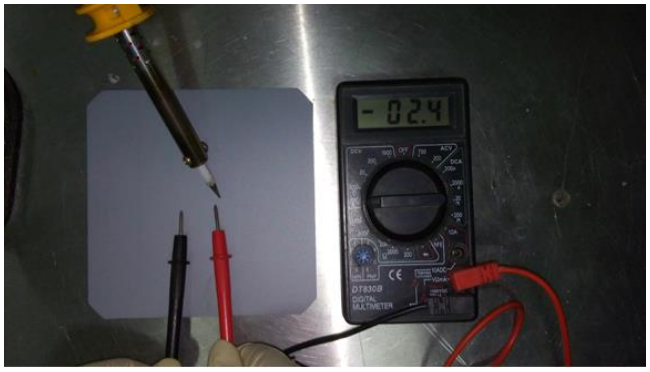

Fig. 6. "Hot-Probe" Experiment

2.3.2 Sheet Resistance Measurement

The sheet resistance is an electrical parameter which describes the current conductivity of thin films of conducting and semiconducting materials. Sheet resistance was determined after layer deposition by directly using four-point probe measurement equipment for quality assurance. If the thickness of the semiconducting layer is not known then the

sheet resistance is specified in Ω/sq. Otherwise, it is called sheet resistivity and the unit is expressed as Ω.cm. Here, P-type and N-type layers sheet resistivity and sheet resistance were measured using Kithlink four-point probe measurement equipment. Furthermore, from the sheet resistance electron concentration, hole concentration and other parameters were calculated theoretically and tabulated by using the following two equations.

$$\sigma = \frac{1}{\rho} \; ; \ldots\ldots (1) \; [31]$$

$$\sigma = q\,(\mu_n n + \mu_p p) \; ; \ldots\ldots (2) \; [32]$$

Where σ is conductivity, ρ is sheet resistance/resistivity, n is electron concentration (cm^{-3}), p is hole concentration (cm^{-3}), μ_p is hole mobility ($cm^2/v{\cdot}s$), μ_n is electron mobility ($cm^2/v{\cdot}s$) and q is the electron charge in 1.6×10^{-19} coulombs. It is worthwhile to mention that the hole mobility value is considered $450 cm^2/v{\cdot}s$ and electron mobility is considered $1200\ cm^2/v{\cdot}s$ [30].

2.3.3 Elemental Analysis by EDS

Elemental analyses were performed on the semiconductor samples by using AMETEK Octane Prime Energy Dispersive X-Ray Spectroscopy (EDS).The N-type substrate fabricated using 5 min deposition and 10 min drive time shows the best sheet resistance value. Thus, the EDS measurement was taken for that sample with 5kV and 20 kV accelerating voltage. It is expected that, by increasing the accelerating voltage EDS from 5 kV to 20 kV, the electrons of electron gun of EDS goes deeper and gives more in-depth information about the material. Thus, authors used both 5 kV and 20 kV sources for the EDS. Additionally, the EDS measurement of the P-type wafer was also been done.

3. Results and Discussion

3.1 Result of Hot Point Probe Experiment

Interestingly, the "hot point probe" experiment output indicates positive current / voltage reading for all the points on the N-type semiconductor substrates. Like wise, the reverse reading has been observed for all the points on the P-type substrates. Benedict Wen-Cheun Au e*t al.* has also observed similar kind of result [30]. Thus the confirmation of N-type & P-type semiconductor has been made by the "hot point probe" experiment. The physics behind this experiment is that the heat source (soldering iron) causes the charge carriers (electrons in N-type, holes in P-type) to move away from the multimeter lead. That is for the N-type semiconductor substrates, the heat source causes the electrons to flow through the negative multimeter probe and the holes to flow through the positive multimeter probe, thus causing the multimeter reading positive. Conversely for the P-type semiconductor substrates, the multimeter reading becomes negative, since the electrons and holes flow through the positive and negative multimeter probes respectively.

3.2 Result of Four Point Probe Measurement: As stated earlier, according to the specification the P-type wafers resistivity lie between 1-3 Ω.cm. This claim contradicts with the experimentally obtained result. Four-point probe measurement reveals that the sheet resistivity of the both side as-cut P-type silicon substrates remains between 1.12-9.46 Ω.cm. So much variation in the sheet resistance implies that the doping concentration of the substrates are not uniform. Variation in the sheet resistance have also been observed (Table 1) for the N-type doped samples. Therefore, the average value of the sheet resistance has been figured out. It is seen that the highest (65.25 Ω/sq) and the lowest (32.75 Ω/sq) sheet resistance have been achieved for 5 min deposition and 10 min drive time and 20 min deposition and 25 min drive time respectively. In all the cases, the sheet resistance value confirms that the N-type layers have been formed upon the P-type layers.

Table 1. Data for Sheet Resistance

Deposition 5 min and Drive in 10 min		**Deposition 10 min and Drive in 15 min**		**Deposition 20 min and Drive in 25 min**		**Deposition 30 min and Drive in 35 min**	
S1 ρ Ω/sq	**S2 ρ Ω/sq**	**S1 ρ Ω/sq**	**S2 ρ Ω/sq**	**S1 ρ Ω/sq**	**S2 ρ Ω/sq**	**S1 ρ Ω/sq**	**S2 ρ Ω/sq**
50.6	**80.2**	**41.3**	**48.1**	**28.7**	**37.3**	**49**	**61.7**
50.4	**80**	**41.1**	**48.1**	**28.1**	**37.1**	**49.2**	**61.8**
50.4	**79.9**	**41**	**48.1**	**28.6**	**36.7**	**48.9**	**61.7**
Avg. 65.25 Ω/ sq		**Avg. 44.62 Ω/ sq**		**Avg. 32.75 Ω/ sq**		**Avg. 55.38 Ω/ sq**	

Footnotes: S1 & S2 defines Sample 1 & Sample 2. ρ is sheet resistance in Ω/ sq

Table 2. Data for Different Parameter Values of N-type Doped Wafer

Dt & Dr_t	**ρ**	**t**	**Rs**	**n**	**n_i**	**p**
5 & 10	**65.25**	**1**	**0.006525**	**7.98×10^{17}**	**1.5×10^{10}**	**281.9**
10 & 15	**44.62**		**0.004462**	**1.17×10^{18}**		**192.3**
20 & 25	**32.75**		**0.003275**	**1.59×10^{18}**		**141.5**
30 & 35	**55.38**		**0.005538**	**9.4×10^{17}**		**239.4**

Footnotes: D_t is deposition time and Dr_t is drive time in min, ρ is sheet resistance in Ω/ sq, t is thickness in μ.m. , Rs is sheet resistivity in Ω -cm, q is electron charge in coulombs, $\mu_p$is hole mobility in $cm^2/v{\bullet}s$, $\mu_n$is electron mobility in $cm^2/v{\bullet}s$, n is electron concentration in cm^{-3}, $n_i$is intrinsic carrier concentration in cm^{-3} and $p=(ni)^2/n$ is hole concentration in cm^{-3}.

Table 2 shows the calculated parameter values of the N-type doped wafers. For the N-type doped wafers the maximum and the minimum values of the electron concentrations are found 1.59×10^{18} cm^{-3} and 7.98×10^{17} cm^{-3} respectively. Therefore, the inference is that the electron concentration falls in the moderate to heavy doping range [33].

Interestingly, by observing both Table 1 and 2 it is found that the sheet resistance decreases and the electron concentration increases for a period of maximum 20 min deposition time and 25 min drive time. Thus it can be assumed that in general, increasing the diffusion time will decrease the sheet resistance value as well as will increase the electron concentration level. Surprisingly, this assumption is not applicable for 30 min deposition time and 35 min drive time. In this case, the sheet resistance value is found higher. This may be due to the formation of the dead layer. Due to high diffusion and drive time, the high phosphorus concentration causes to form an electrically inactive phosphorus layer called a dead layer on the silicon surface. The dead layer increases the sheet resistance and thus hinders the performance of a solar cell [34-35].

The relationship between how defects in the Si crystal is affected by the diffusion and drive time is observed also. Impurity defects (classification of Point Defect) is introduced by phosphorus diffusion and drive time. By increasing 5 min deposition and 10 min Drive time to a period of maximum 20 min deposition and 25 min drive time allows shallow donors to increase form 7.98×10^{17} cm^{-3} to 1.59×10^{18} cm^{-3}. Thus sheet resistance is reduced and conductivity is increased. It seems that, adding small amounts of impurity defects by phosphorus diffusion and drive time allows some control of the conductivity of the semiconductor. However, as deposition time is increased to 30 min and drive time to 35 min, dead layer is formed, and it functions as a defect degrading the electrical performance of the emitter. Other defects may be also introduced but are beyond the scope of this paper and is wished to be discussed in future work.

As stated in the literature, the standard solar cell sheet resistance range is between 40 Ω/sq - 90 Ω/sq. Among all the samples, the sheet resistance of the N-type layers fabricated using 5 min deposition and 10 min drive time has the required sheet resistance that falls in between 40 Ω/sq - 90 Ω/sq. In addition, considering minimum utilization of gases, values of sheet resistance and carrier concentration 5 min deposition and 10 min drive time provides the most suitable diffusion recipe to fabricate the N-type layer on the P-type layer.

3.3 Elemental Analysis

The EDS spectrum of P-type silicon wafer is shown on the Figure 7. The X-axis reperents the accelerating voltage of electron gun Energy in (keV) and the Y-axis reperents the counts per second per eV. Higher the counts of a particular element, higher will be its presence at that point or area of interest. EDS system software has been used to analyze the energy spectrum in order to determine the abundance of specific elements. ZAF correction has also been applied. Weight % and Atomic % has been calculated and tabulated in Table 3.

The data obtained by EDS (Table 3) shows that the P-type wafer is composed of Boron (B) and Silicon (Si). The presence of Boron (B) and Silicon (Si) confirms that it is indeed P-type doped silicon wafer.

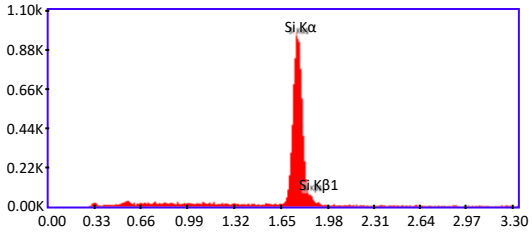

Fig. 7. EDS Spectrum of P-type Doped Silicon Wafer

Table 3. EDS Data for P-type Wafer

Element	Weight %	Atomic %
B	0.6	1.5
Si	99.4	98.5

The EDS spectrum has been also been obtained for (Figure 8 and Figure 9) the N-type substrate fabricated using 5 min deposition and 10 min drive time with 5 kV and 20 kV accelerating voltage. Again EDS system software has been used to calculate the Weight % and Atomic % of the matrials preneted in the the N-type substrate. The Weight % and Atomic % of the N-type substrate has been tabulated in Table 4. The EDS data reveals that (Table 4) Boron (B), Oxygen (O), Phosphorus (P) and Silicon (Si) are found in the fabricated N-type layer with 5 kV accelerating voltage. The presence of Boron (B) indicates that complex Boron – Oxygen defect is present in the newly formed N-type layer [38-39]. The Boron – Oxygen defect was first reported in 1973 by Fischer and Pschunder [40]. However, when the accelerating voltage of EDS was increased up to 20 kV, then the presence of Boron was not observed. Thus it is expected that Boron – Oxygen defect will not affect the performance of solar cell that much. Existence of Phosphorus (P) indicates that the N-type layer has been formed. Furthermore, Oxygen in the N-type layer suggests that surface passivated layer has been grown upon the N-type layer. Also, the concentration of oxygen is found higher for 5 kV accelerating voltage than 20 kV accelerating voltage. It tells us that, by increasing the accelerating voltage, the electrons of electron gun of EDS goes deeper and gives more in-depth information about the material. David Cohen-Tanugi and Nan Yao also found that raising the accelerating voltage of EDS, increases the penetration depth of electron in the material [41]. Additionally, the surface passivated layer thickness decreases as penetration depth of electron increases (by observing Oxygen's percentage, Table 4).

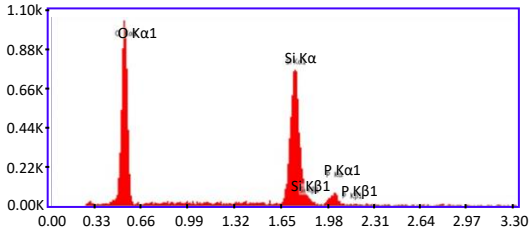

Fig. 8. EDS Spectrum of N-type Doped Silicon Wafer (accelerating voltage 5 kV)

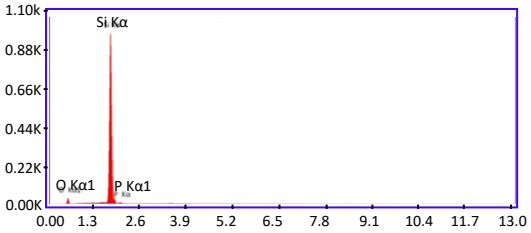

Fig. 9. EDS Spectrum of N-type Doped Silicon Wafer (accelerating voltage 20 kV)

Table 4. EDS Data for *N*-type Wafer (5 min Diffusion and 10 min Drive-in)

	5kV (Accelerating voltage)		20 kV (Accelerating voltage)	
Element	Weight %	Atomic %	Weight %	Atomic %
B	0.4	0.9	0.0	0.0
O	36.1	49.8	15.9	25.0
Si	56.0	44.0	82.4	73.7
P	7.4	5.3	1.7	1.3

3.4 Physics behind the N-type Layer Formation

By observing the hot point probe experiment, sheet resistance value and EDS data, it is confirmed that the N-type layers are indeed formed upon monocrystalline both side as-cut P-type wafers, and it is accomplished the reactions among different gases in the deposition and drive-in stage. The reactions of the deposition stage are shown in the following equations [42]:

$$\mathbf{POCl_3\ (liquid) + N_2\ (bubble) \rightarrow POCl_3\ (vapor)} \quad \ldots\ldots (3)$$

$$\mathbf{4POCl_3\ (vapor) + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2} \quad \ldots\ldots (4)$$

At first in the deposition stage, the Nitrogen gas flows through liquid Phosphorus Oxychloride ($POCl_3$) and produces Phosphorus Oxychloride vapor (eq.3).Which reacts with oxygen and forms Phosphorus Pentoxide (P_2O_5) (eq.4).

$$\mathbf{2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2} \quad \ldots\ldots (5)$$

$$\mathbf{P + 3Si \rightarrow N - type\ doped\ Si} \quad \ldots\ldots (6)$$

Then, in the drive-in stage, the P_2O_5 immediately reacts with the silicon (eq. 5). The P_2O_5 acts as an infinite source for phosphorous diffusion resulting in, in-diffusion of phosphorus and causes the formation of the phosphosilicate glass (PSG) (eq.6). The phosphosilicate glass is normally etched off using dilute hydrofluoric acid but has not been done in this case.

Keeping in mind the fact of cost-effectiveness, based on the work of Cuevas *et al.* thermal oxidation was adopted to remove the dead layer over the PSG rather than chemical etching process [43-46]. Again, Oxidation is a preferable process as it enhances phosphorus diffusion [47-48]. Furthermore, thermal oxidation causes surface passivation which reduces the number of dangling bonds thus reducing the recombination effects and enhances the performance of solar cell [49-50]. Thus by the application of O_2 gas in the thermal oxidation stage, the SiO_2 layer grows upon phosphosilicate glass (PSG) and overall N-type layer forms upon the monocrystalline as-cut P-type wafer.

4. Conclusion

In this research, the formation of N-Type layer upon monocrystalline P-type silicon wafer using $POCl_3$ diffusion process has been comprehensively discussed. A thorough study on the literature reveals that the deposition and drive time during diffusion process is not fixed. Therefore, to find out the optimum deposition and drive time, various combinations of these two timings were experimented.

Furthermore, focus has been given to reduce the cost of N-type layer fabrication and to have a standard sheet resistance value of 40 Ω/sq - 90 Ω/sq. In addition, both side as-cut P-type silicon wafers have been used as-cut P-type substrates instead of polished P-type silicon wafers. Furthermore, based on the work of Cuevas *et al.* thermal oxidation has been applied after diffusion process. Overall at 875°C N-type layers have been grown in an $POCl_3$ diffusion furnace by utilizing $POCl_3$ N_2 and O_2 gas. Moreover, three types of characterization such as N-type and P-type semiconductor determination, sheet resistance measurement and elemental analysis by EDS were done. Hot probe test identifies P-type wafers as well as confirms that in all the cases N-type layers have been formed upon the as-cut P-type monocrystalline silicon wafers. Experimentally measured EDS & sheet resistance data also verifies that N-type layer has been formed. EDS measured data also reveals that surface has been passivated due to thermal oxidation. Among all the samples, the sheet resistance of the N-type layer fabricated using 5 min deposition and 10 min drive time has the best sheet resistance of 65.25 Ω/ sq with electron concentration 7.98×10^{17} cm^{-3}. The cost reduction has been done by decresing the deposition time (less utilization of $POCl_3$ gas) and compensating it with increased drive time (more exploitaion of low cost N_2 gas). Finally, 5 min deposition and 10 min drive time provides the optimum duffusion time and low cost procedure for the creation of N-Type layer over monocrystalline both side as-cut P-type silicon wafer and it is proposed to be used for the solar cell industry.

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